

B450 AORUS PRO WIFI

PAGE TITLE *Revision : 1.01*

01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	CPU DDR4 MEMORY
05	CPU CONTROL
06	CPU GFX, GPP, SB, GND
07	CPU ACPI/GPIO/USB/AUDIO
08	CPU POWER & GND
09	CPU CLK/SPI/USB
10	DDR4 CHANNEL A
11	DDR4 CHANNEL B
12	PM CLK, SPI, MISC
13	PM USB
14	PM UMI/GPP/SATA
15	PM POWER & GND
16	PCI EXPRESS x16
17	HDMI , DVI
18	IT8688CX , TPM
19	F_USB30 , R_USB30 , F_USB20
20	A_VDD1V8
21	ALC1220 CODEC
22	AUDIO JACK
23	POWER SEQUENCE , A_VDDP
24	PWM SL95712
25	VCORE MOS , VCORE_SOC MOS

<https://vinafix.com>

PAGE	TITLE
26	ATX , F_PANEL
27	PM PWR,VDDA25, VCC11DUAL
28	DDR POWER , 5VDUAL
29	Intel I211AT LAN
30	FAN
31	M.2 , SWITCH
32	PCIEx4 , PCIEx1
33	BOTTOM
34	TOP, PCIE x1
35	CPU / IO / DDR / C_ LED
36	PCB / AUDIO LED
37	IT8792 EC1
38	D_LED
38	M2B SOCKET
40	TYPE C

GIGABYTE™

Title

COVER SHEET

Size

Custom

Document Number

B450 AORUS PRO WIFI

Rev

1.01

Date

Wednesday, September 26, 2018

Sheet

1

of

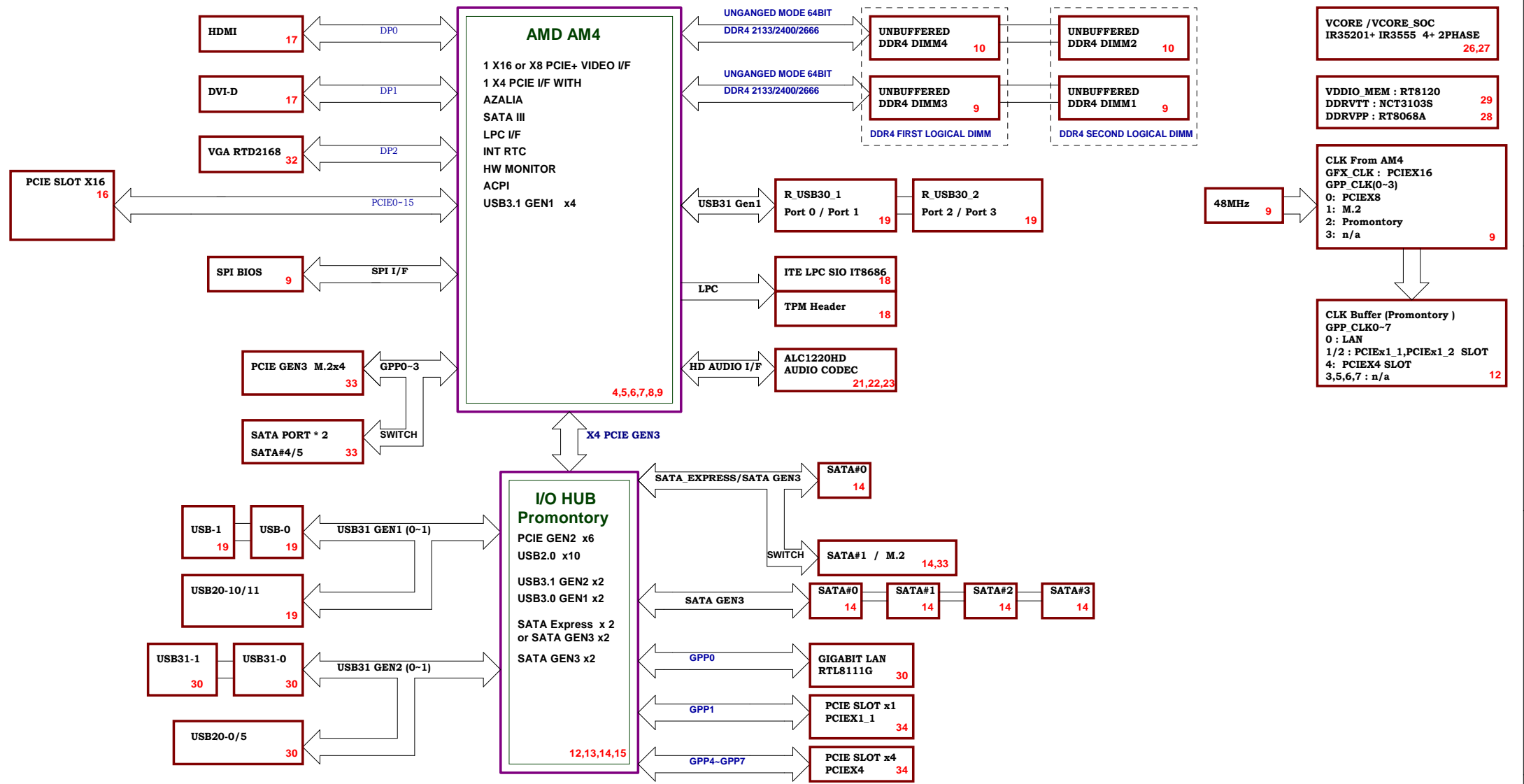
40

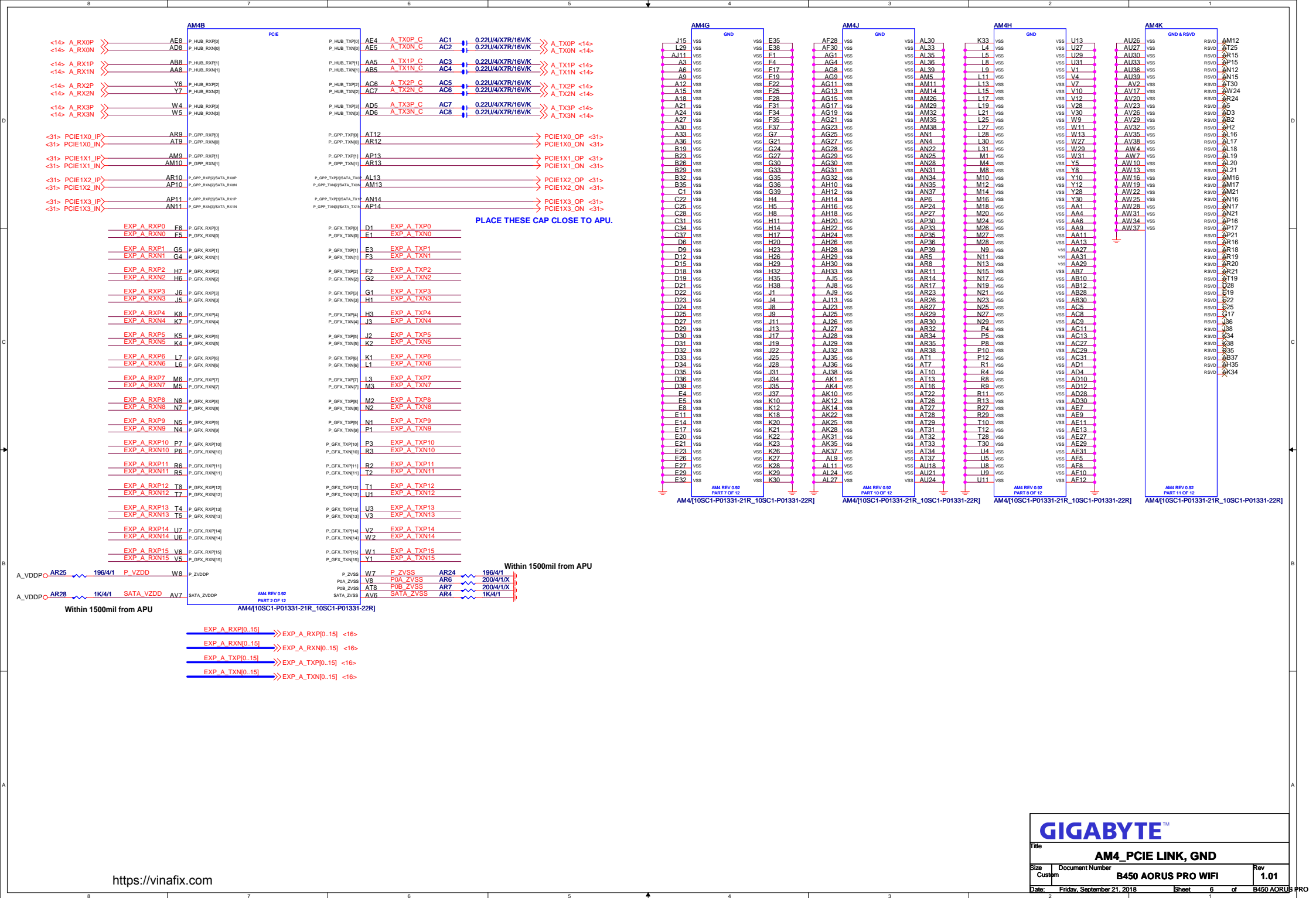
2015.12.30~B.L

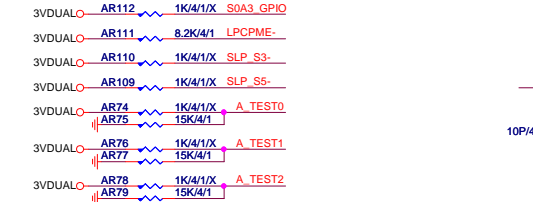
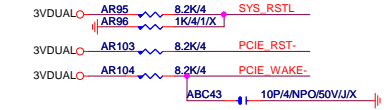
[illegible][illegible][illegible]

	S		4		3		2		1							
	Model Name:B450 AORUS PRO WIFI															
	Component value change history				Version: 1.01											
					P-Code: U98126-0											
D																
C																
B																
A																

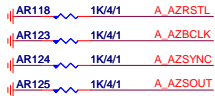
[illegible][illegible][illegible][illegible][illegible]



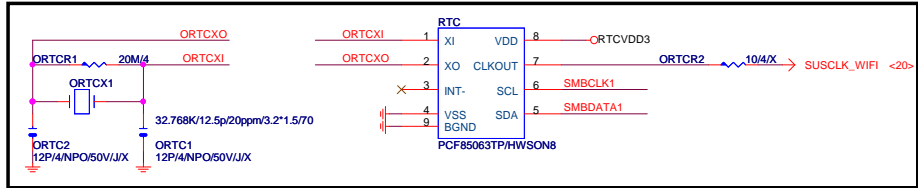
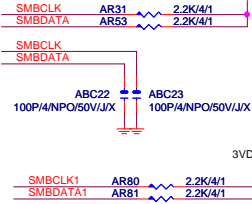
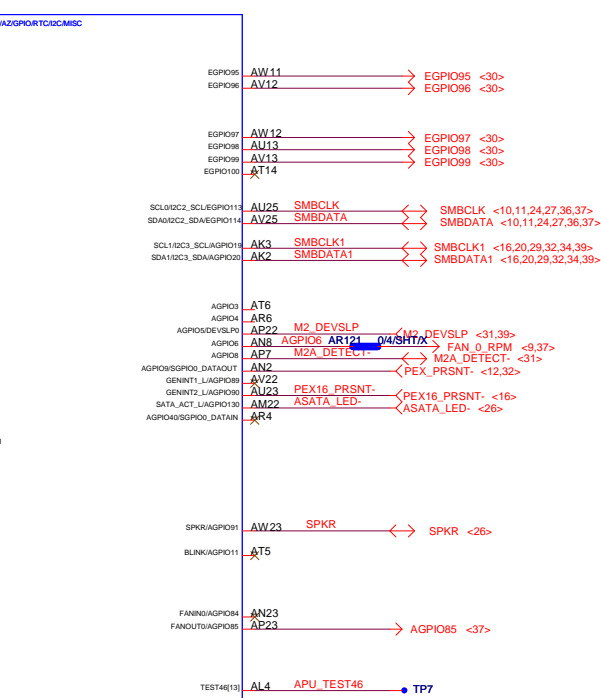
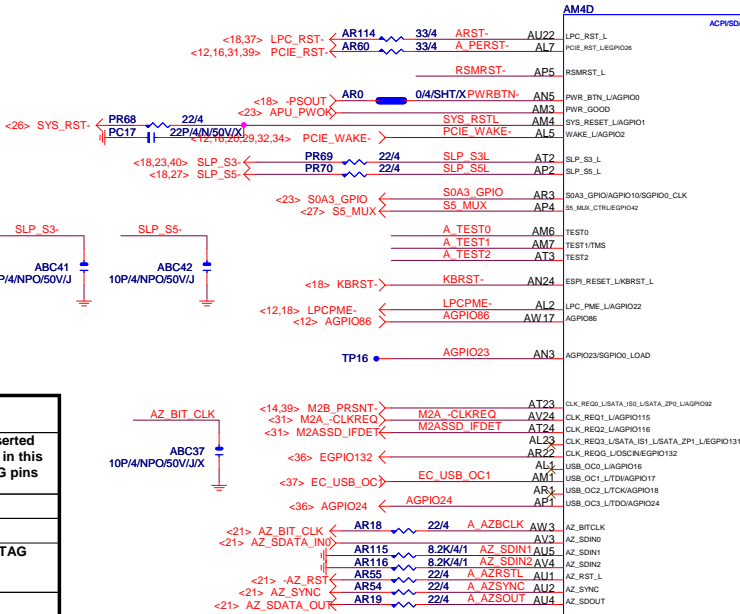




Internal Debug Only			
TEST0	TEST1	TEST2	Description
0	0	0	FCH TAP accessible from APU when TAPEN is asserted FCH JTAG pins overloaded for multiple functions, in this configuration the FCH JTAG are used as non-JTAG pins
0	0	1	Reserve
0	1	X	Reserve
1	TMS	0	FCH JTAG multi-function pins are configured as JTAG pins, in this configuration the FCH TAP can be accessed from FCH JTAG pins
1	TMS	1	Use on JTAG only, Yuba JTAG enable.



	LPC_CLK0	LPC_CLK1	AGPIO3	RTC_CLK	LFRAME_L	SYS_RST#	SPI_CLK (ZP)
PULL HIGH	BOOT FAIL TIMER ENABLED	Use 48MHz crystal clock and generate both internal and external clocks (DEFAULT)	Enhanced reset logic (for quicker S5 S5 resume) (DEFAULT)	Coin battery is on board. (DEFAULT)	SPI ROM (DEFAULT)	normal reset mode (DEFAULT)	Use 48MHz crystal clock and generate both internal and external clocks (DEFAULT)
PULL LOW	BOOT FAIL TIMER DISABLED (DEFAULT)	Use 100MHz PCIE clock as reference clock and generate internal clocks only	Default to traditional reset logic (DEFAULT)	Coin battery is not on board.	LPC ROM	short reset mode	Use 100MHz PCIE clock as reference clock and generate internal clocks only
CP/ST DIE ONLY https://vinafix.com						ZP DIE ONLY	

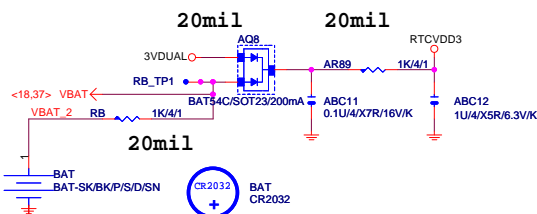


GIGABYTE™

Title
AM4 MISC

Size Custom Document Number
B450 AORUS PRO WIFI Rev
1.01

Date: Friday, September 21, 2018 Sheet 7 of B450 AORUS PRO



A_VDDIOA

AR63 0/4/X

AR47 0/4/SHT/M/X

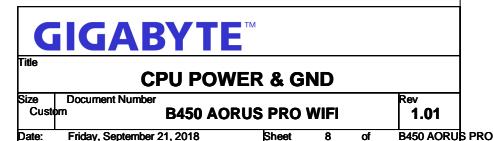
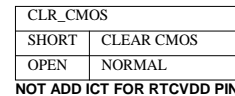
A_VDD1V8

A_VDD18S5

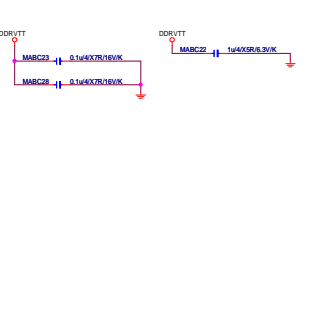
A_BC6

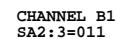
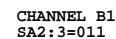
CHECK

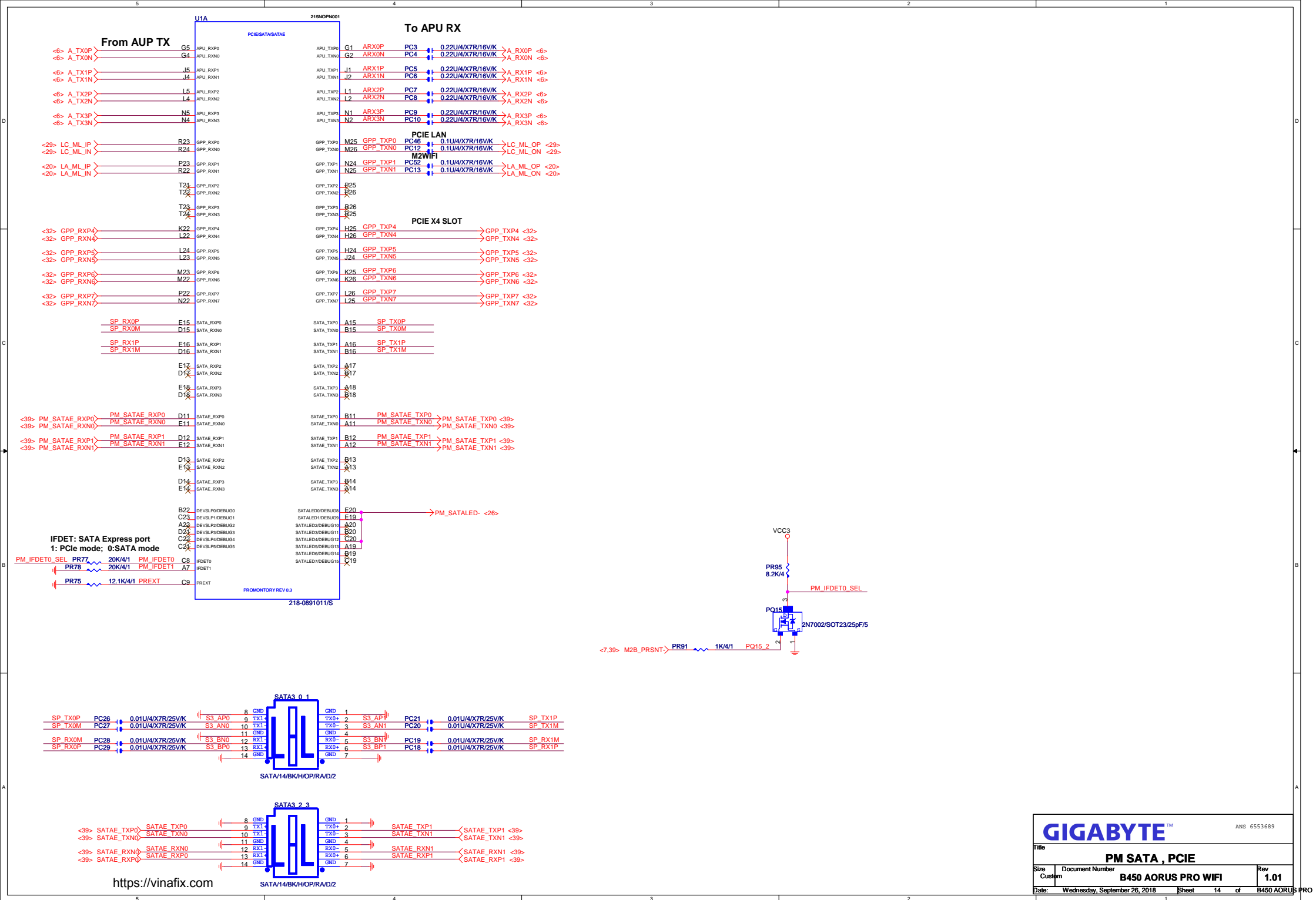
AM4 1.5V, 250mA (A_V15S5)
A_Q1 改接A_VDD18S5 for VDDIO_AUDIO

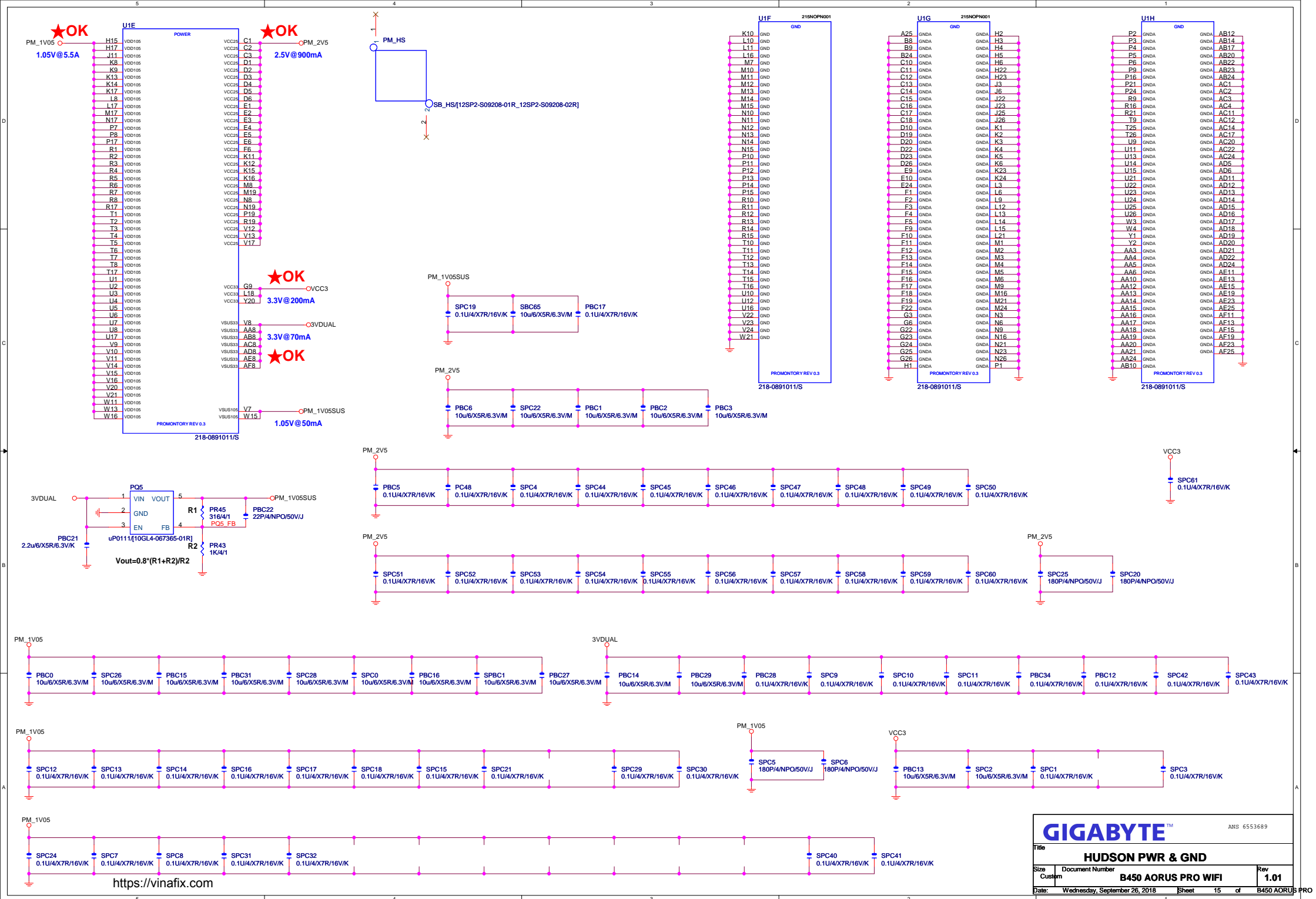


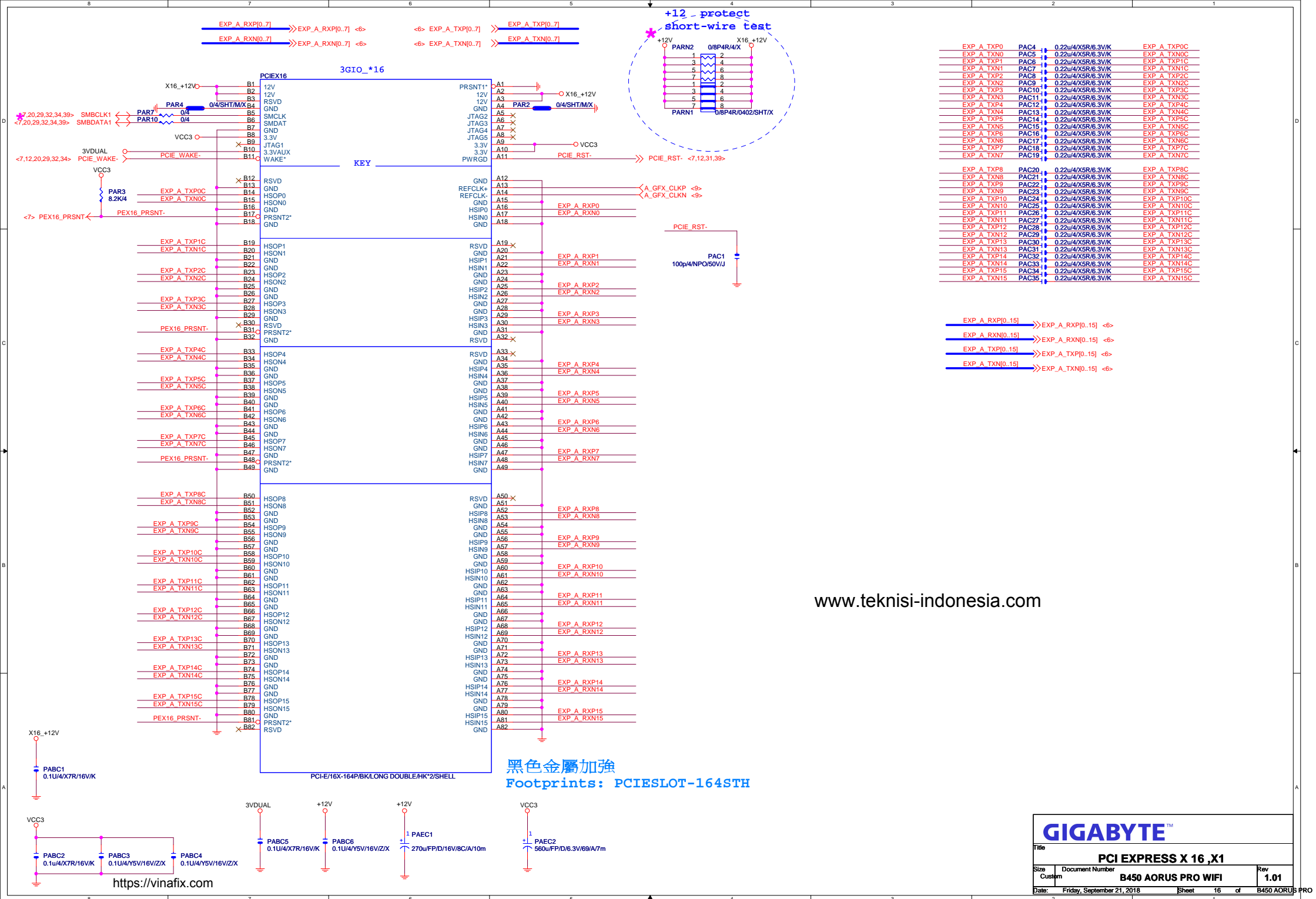


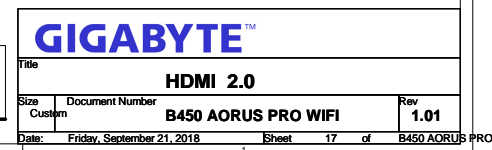
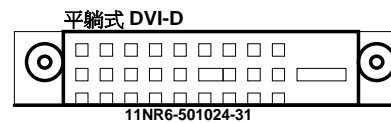
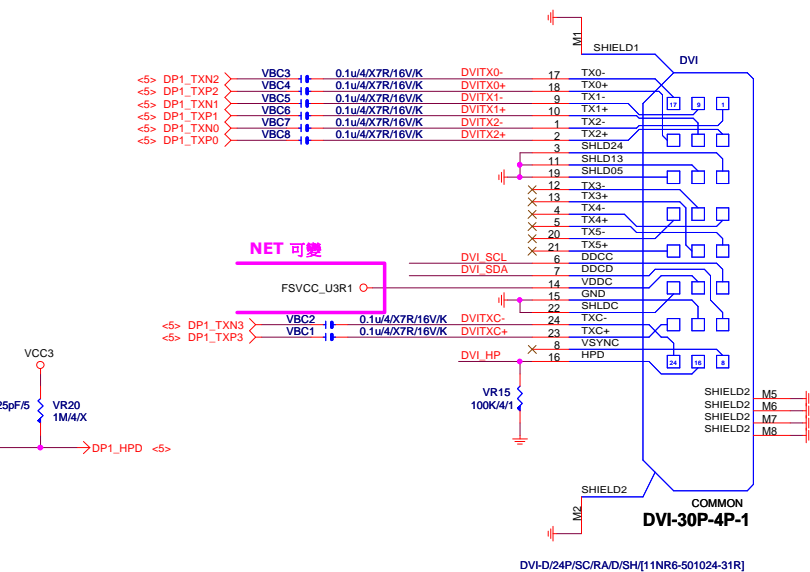
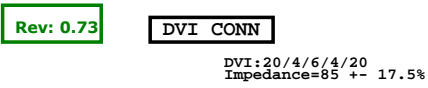
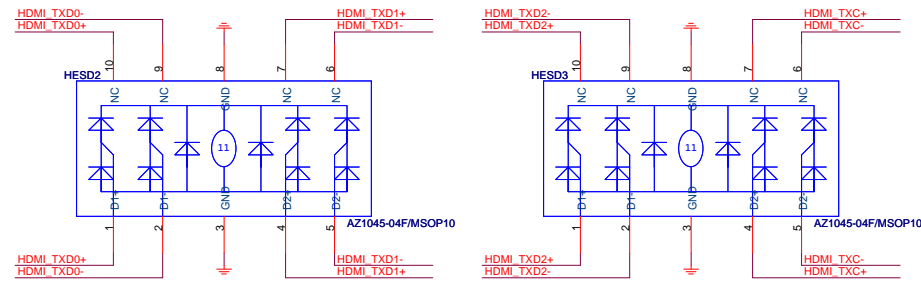
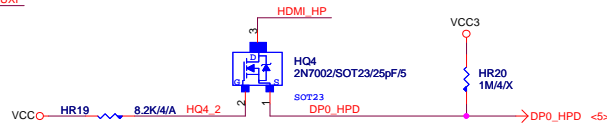


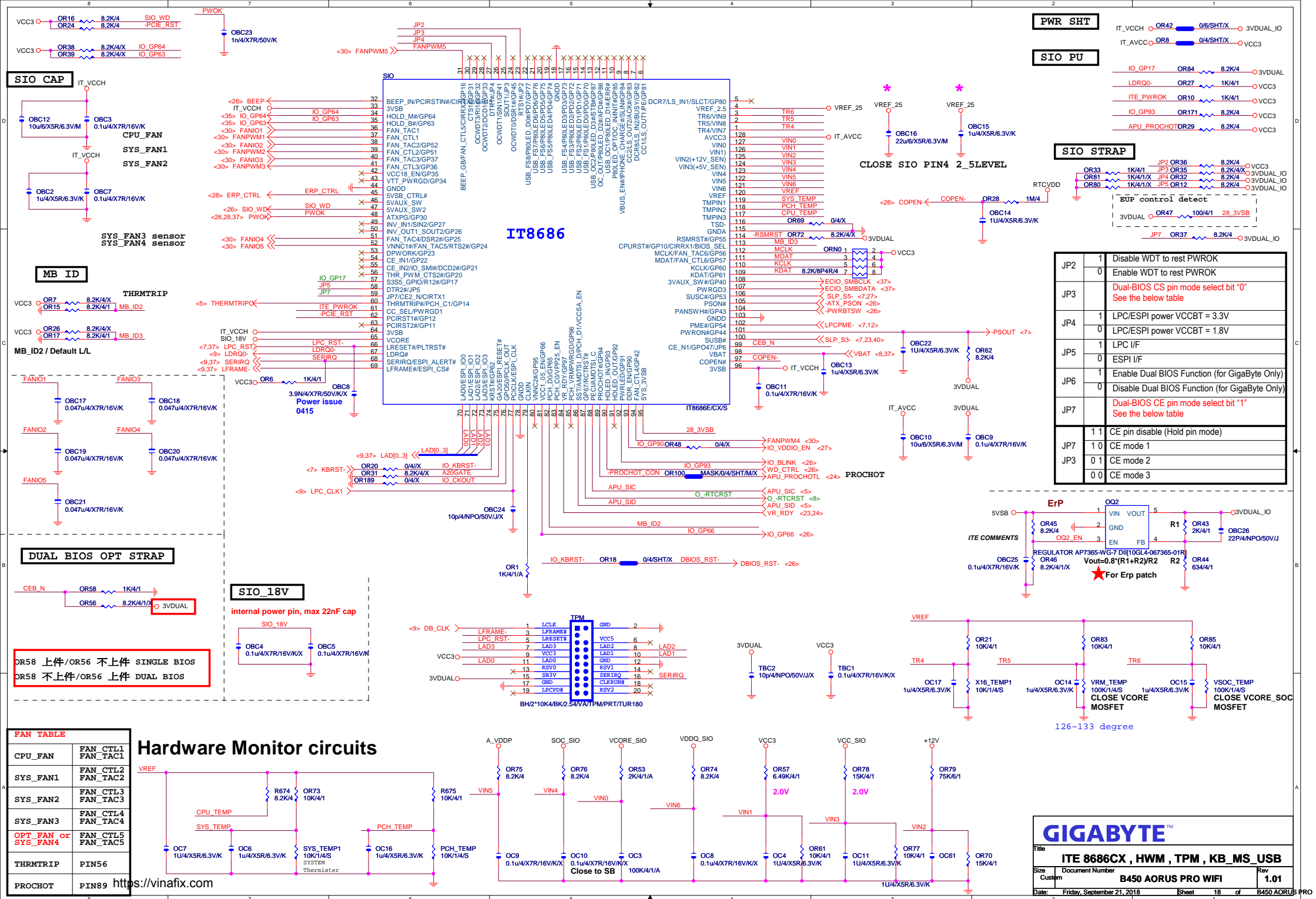




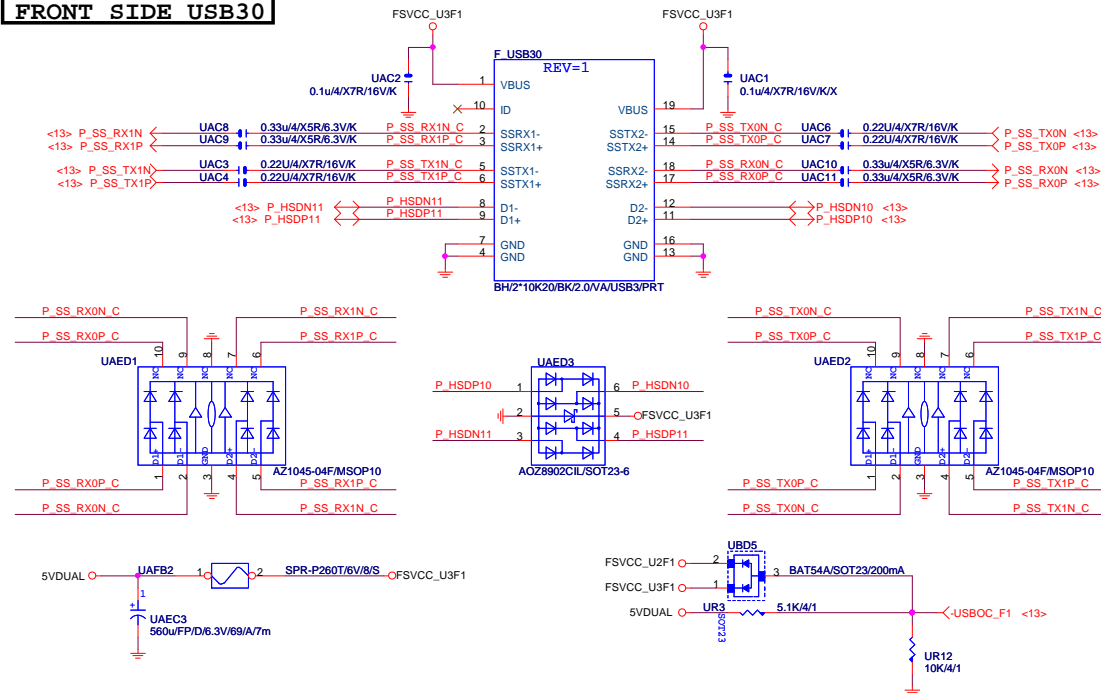




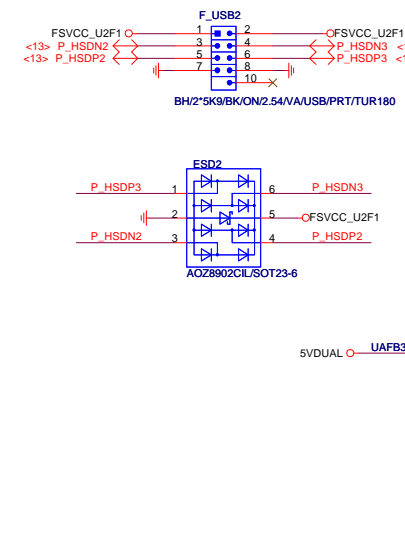




FRONT SIDE USB30



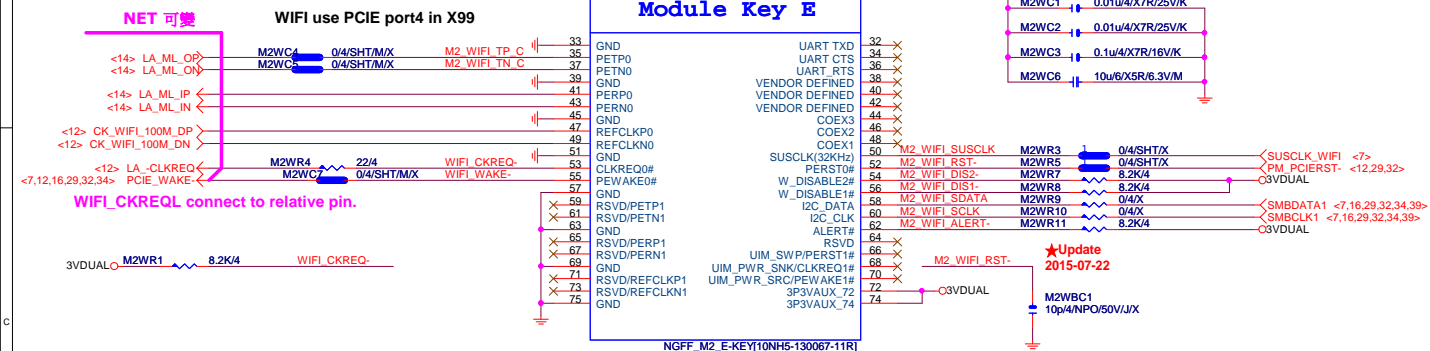
FRONT SIDE USB2



請選擇適用的USBport：
SOC/UD7/UD5/G1/G7：USB4
;UD3/G5:USB6

PCIE:15/4/4/15(breakout min 8/4/4/8)
外層Impedance=85 +- 17.5%

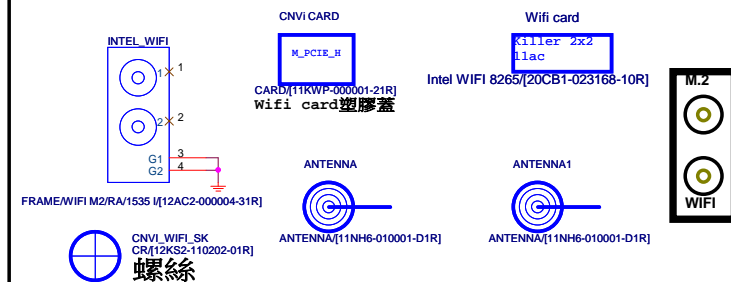
PCIE:15/4/4/4/15(breakout min 8/4/4/4/8)
内層 Impedance=85 +/- 12%



teknisi-indonesia.com

★Update 2015-02-11

一套WIFI MODULE包含外框+WIFI CARD+天線



Footprint Notice.

★Update
2015-07-22
★Footprint
for 直立式
SMD:
WIFI-EKEY

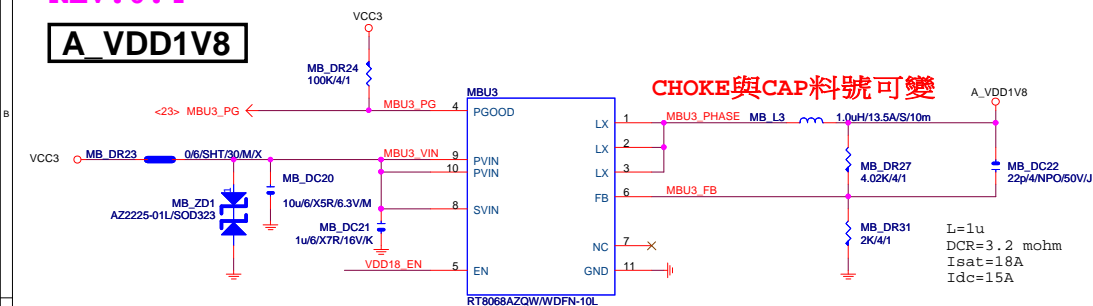
Footprint Notice.

★Update
2015-07-22
★Footprint for
橫躺式SMD: NGFF-E-75P-2

兩片式WIFI金屬殼改為單件式
Layout Library : wifi-ekey-module-1
Tiptop P/N : 12AC2-000004-31R

REV: 0.4

A VDD1V8



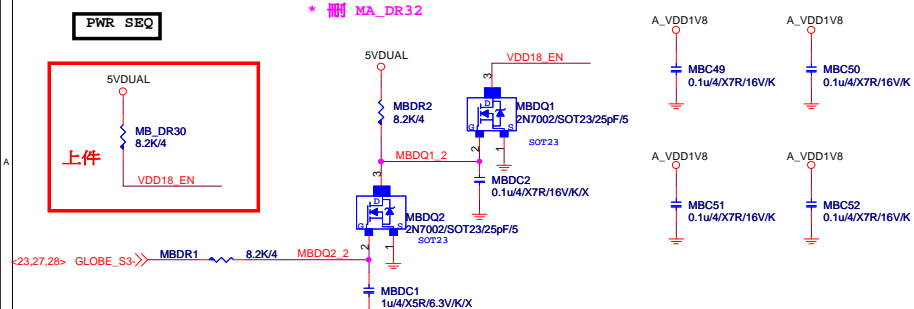
VPP CAP

* 大電容 x0

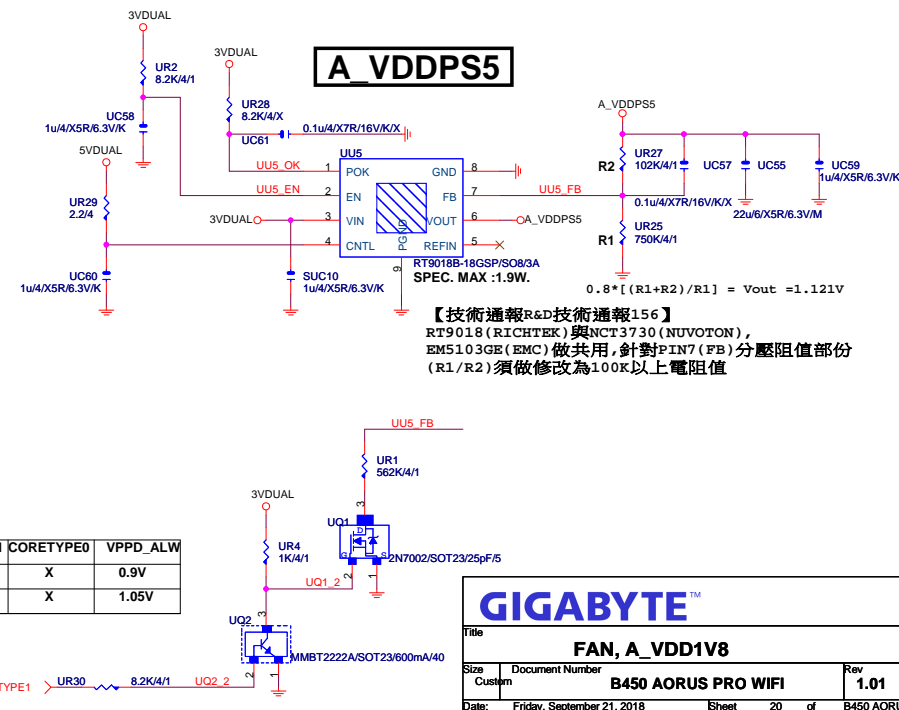
A_VDD1V8

MB_DC23
22u/6/X5R/6.3V/M

22u*1PCS



<https://vinafix.com>



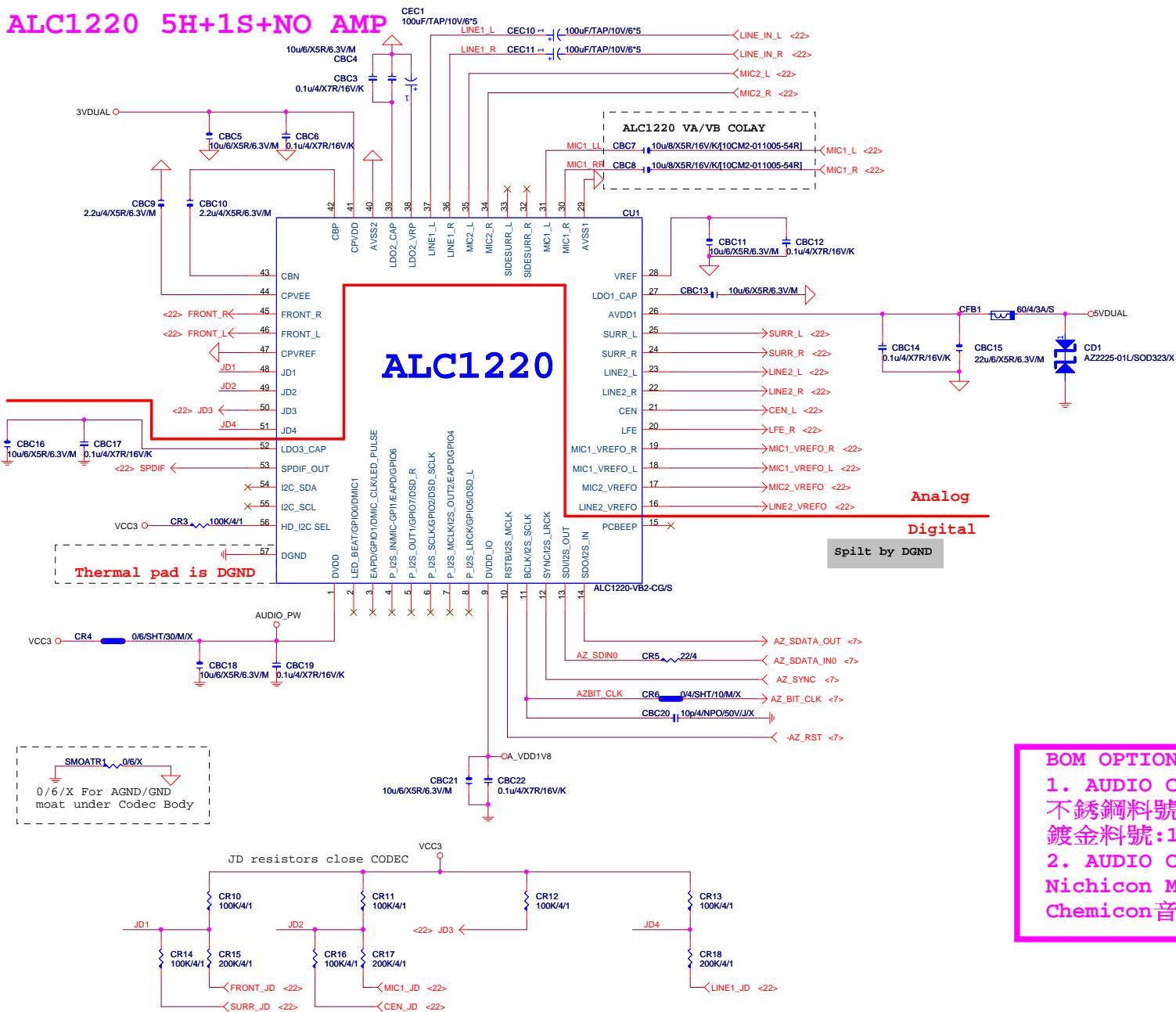
CORETYPE1	CORETYPE0	VPPD_ALV
1	X	0.9V
0	X	1.05V

GIGABYTE

FAN, A_VDD1V8

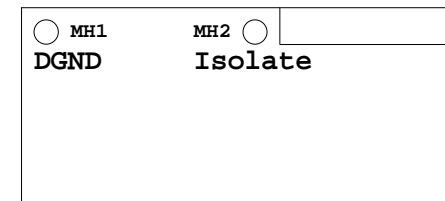
Size	Document Number	Rev
Custom	B450 AORUS PRO WIFI	1.01
Date:	Friday, September 21, 2018	Sheet 20 of B450 AORUS PRO

ALC1220 5H+1S+NO AMP



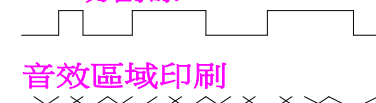
LAYOUT注意:螺絲孔下GND方式

1. MH1下DGND
2. MH2一律改為Isolate



LAYOUT注意:是否要加?

AGND切割線



BOM OPTION :

- ## 1. AUDIO CONNECT

不銹鋼料號:11NR6-403025-A3R

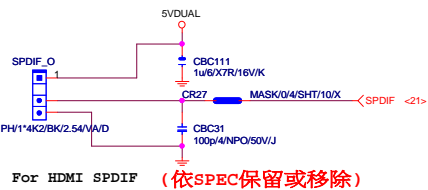
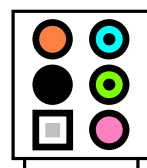
鍍金料號:11NR6-403025-92R

- ## 2. AUDIO CAP

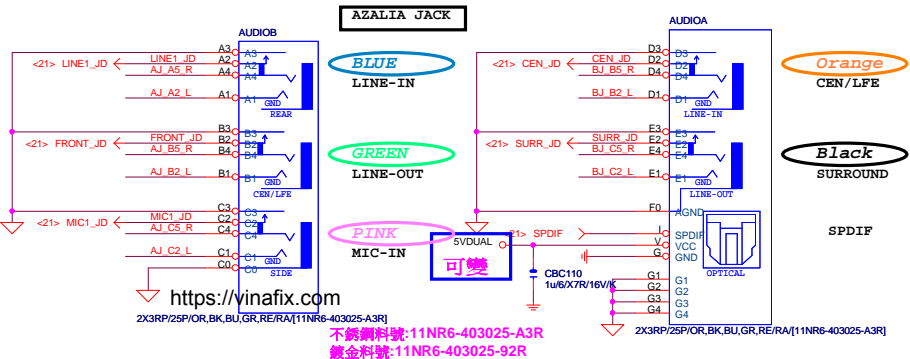
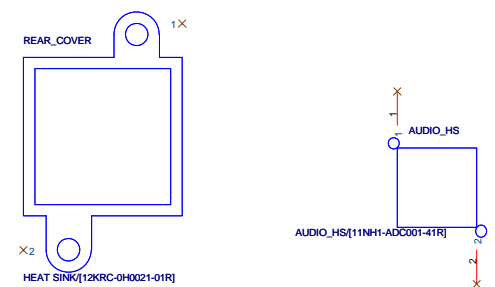
Nichicon MW音效電容 : 11CE1-651000-12R

Chemicon 音效電容：11CE2-651000-05R

AZALIA JACK



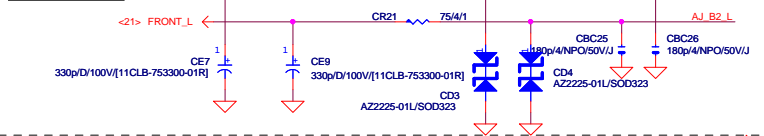
For HDMI SPDIF (依SPEC保留或移除)



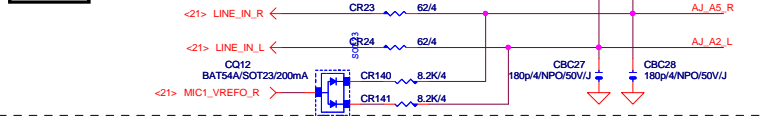
https://vinafix.com

不銹鋼料號:11NR6-403025-A3R
鍍金料號:11NR6-403025-92R

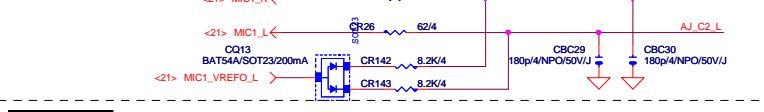
LINE-OUT



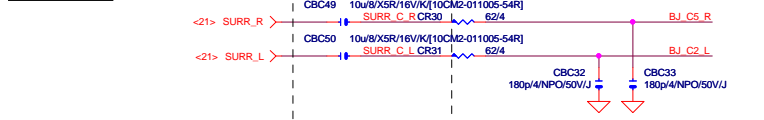
LINE-IN



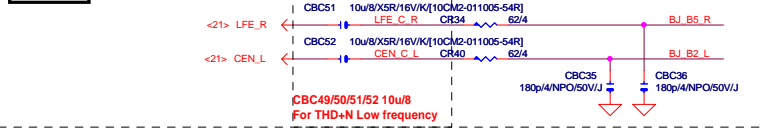
MIC-IN



SURROUND

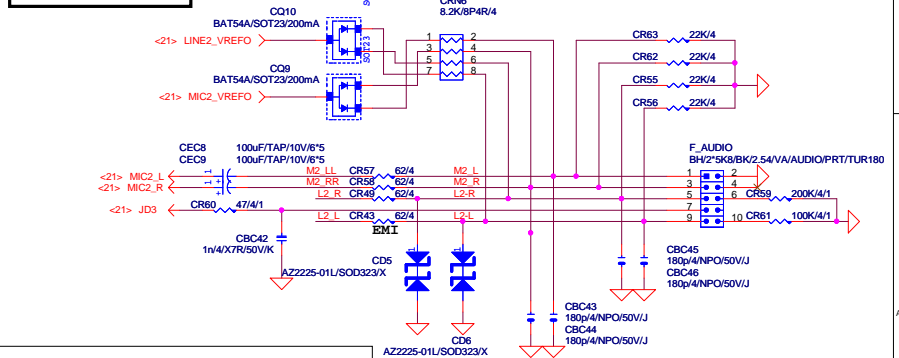


CEN/LFE



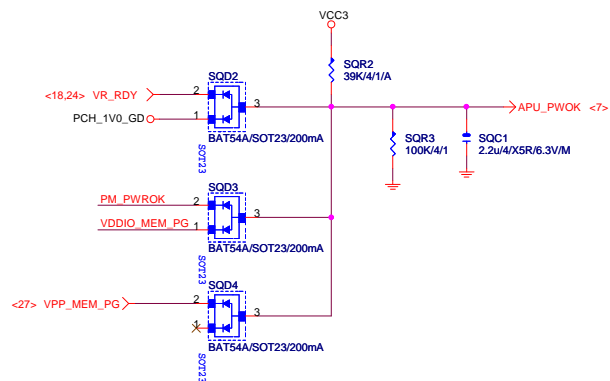
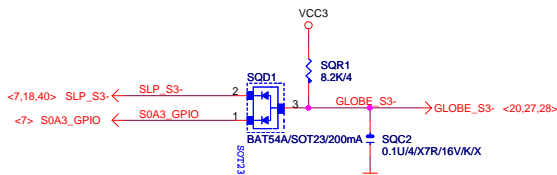
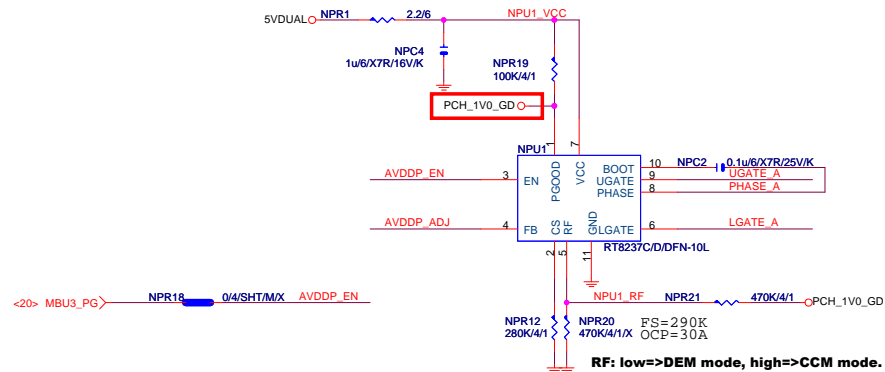
CBC49/50/51/52 10u/8
For THD+N Low frequency

AZALIA FRONT PANE

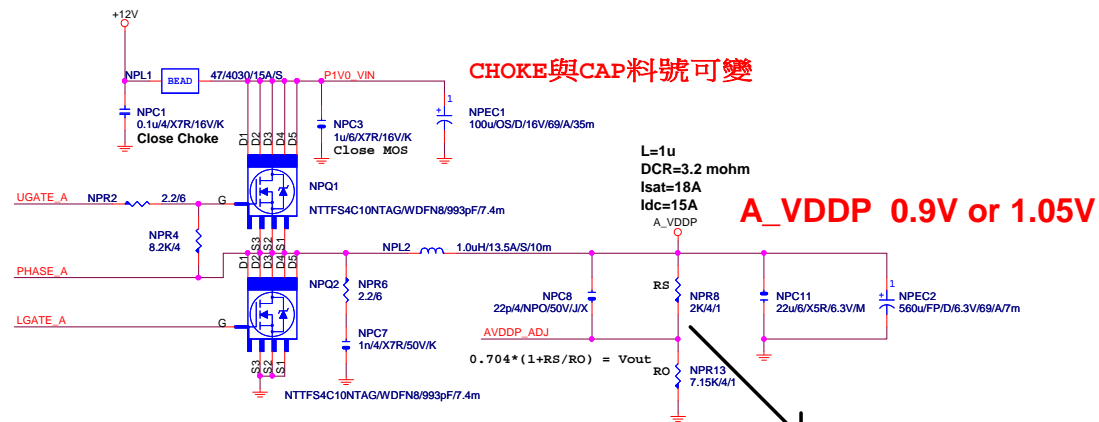


GIGABYTE

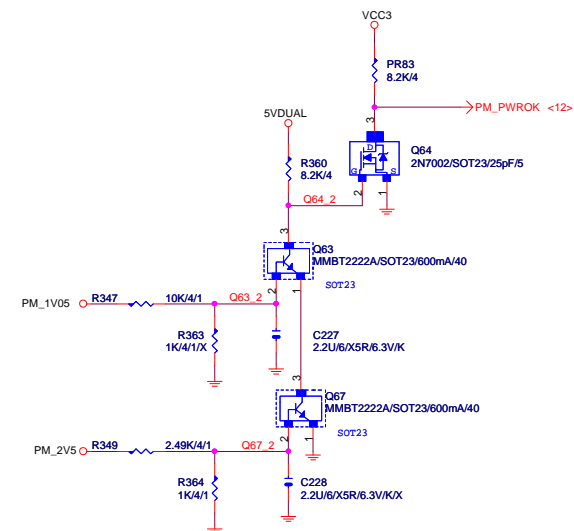
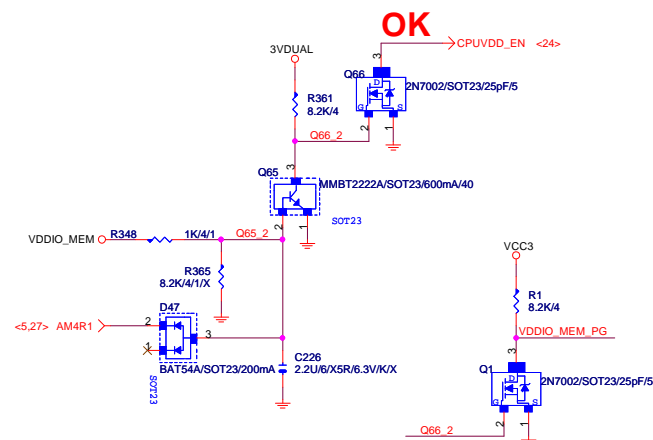
Title			
AUDIO JACK			
Size	Document Number		Rev
Custom	B450 AORUS PRO WIFI		1.01
Date:	Friday, September 21, 2018	Sheet 22 of	B450 AORUS



<https://vinafix.com>



CORETYPE1	CORETYPE0	VPPD_ALW
1	X	0.9V
0	X	1.05V

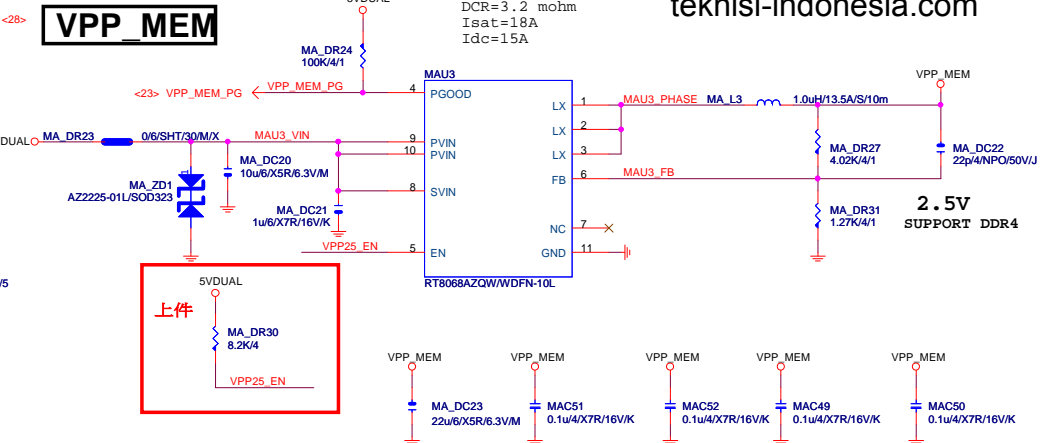
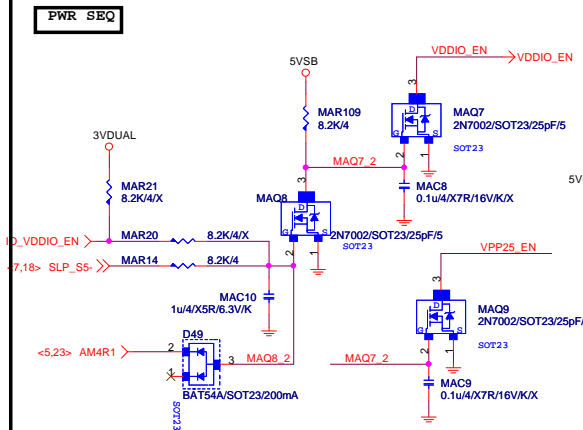
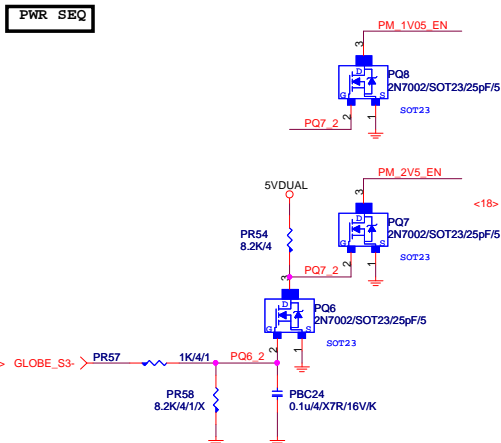
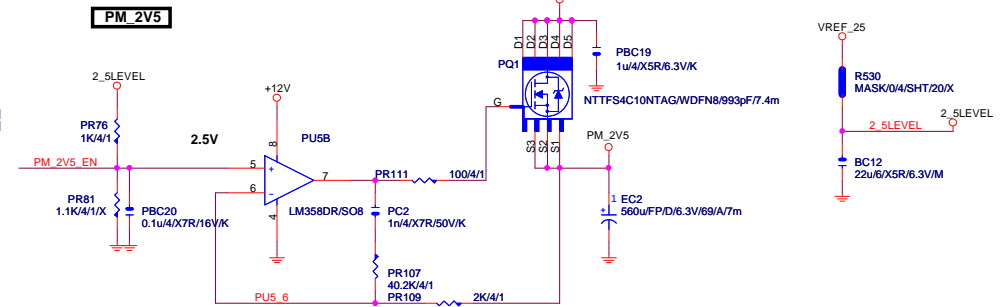
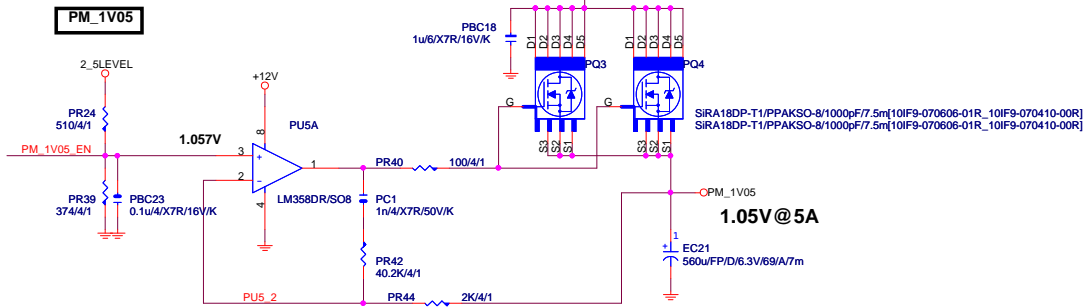


GIGABYTE

POWER SEQUENCE

Size	Document Number	Rev
Custom	B450 AORUS PRO WIFI	1.01

Date: Friday, September 21, 2018 Sheet 23 of B450 AORUS PRO

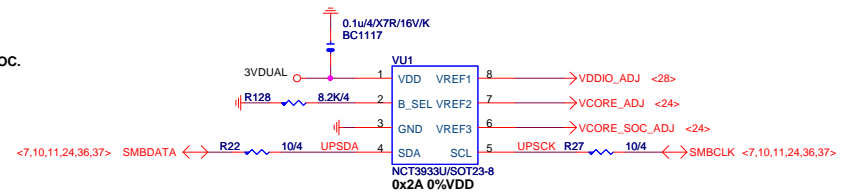


VDDCR SOC S5

S5_MUX: S0-->High, S5-->Low
H: VDDCR_SOC_S5 will track VCore_SOC.
L: If VCore_SOC < 0.775V (OR 0.85V) , VDDCR_SOC_S5=0.775V.
If VCore_SOC>=0.775V (OR 0.85V) , VDDCR_SOC_S5 will trace VCore_SOC.

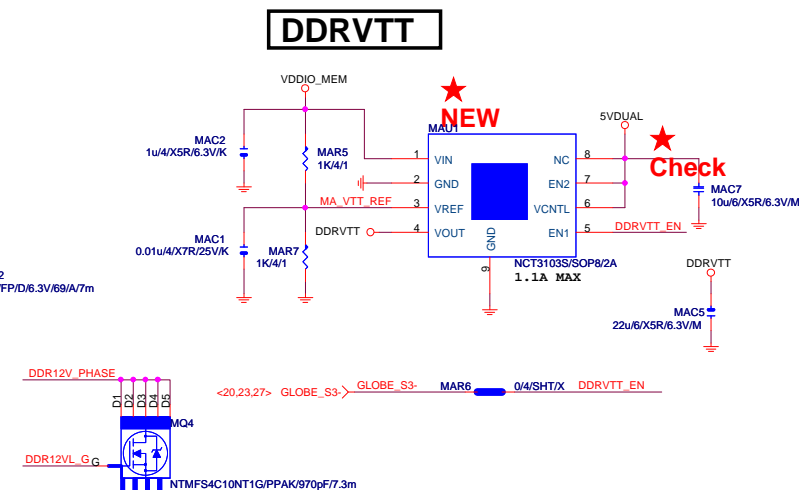
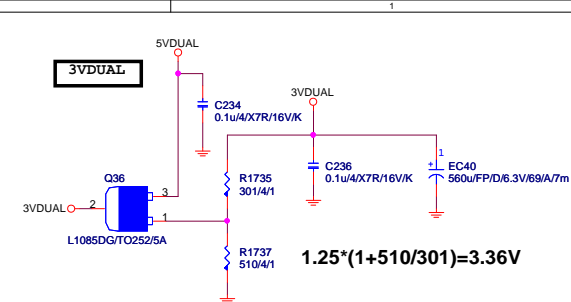



AM4 S5: 0.775V, 200mA,
S0:VAR, 900mA.



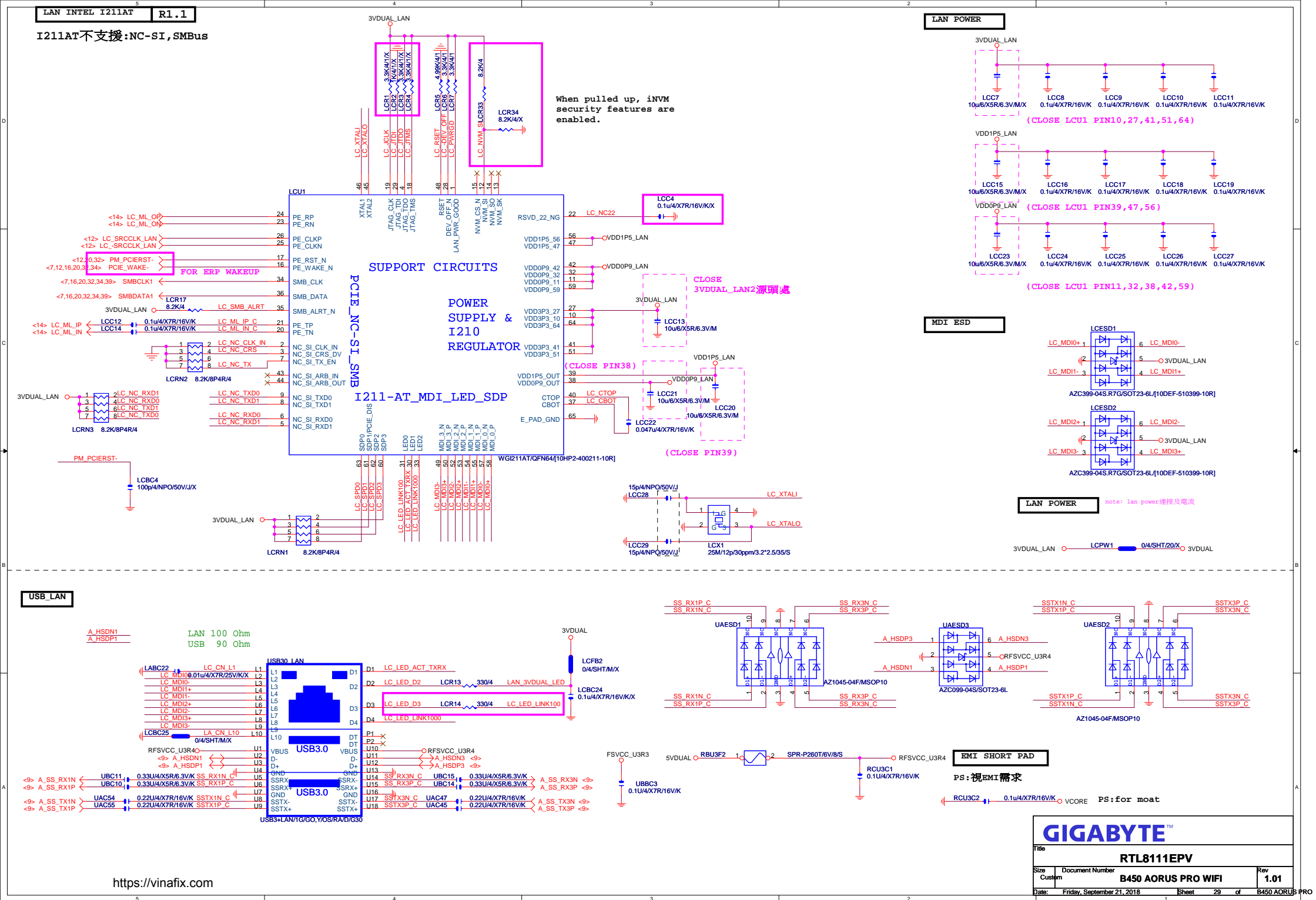
GIGABYTE

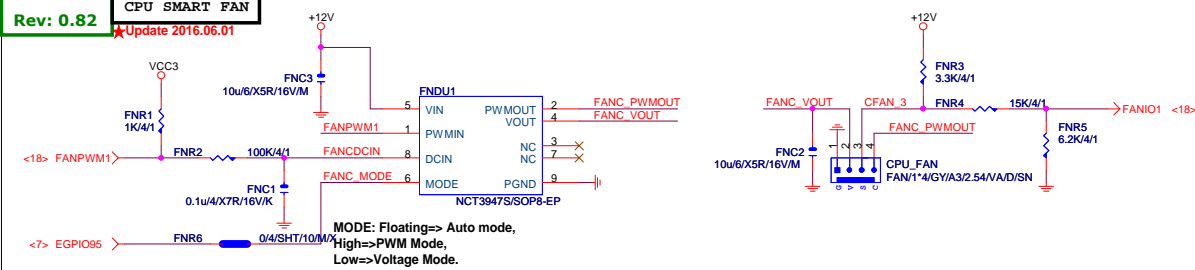
Title			
PM POWER			
Size	Document Number	Rev	
Custom	B450 AORUS PRO WIFI	1.01	
Date:	Friday, September 21, 2018	Sheet	27 of B450 AORUS PRO



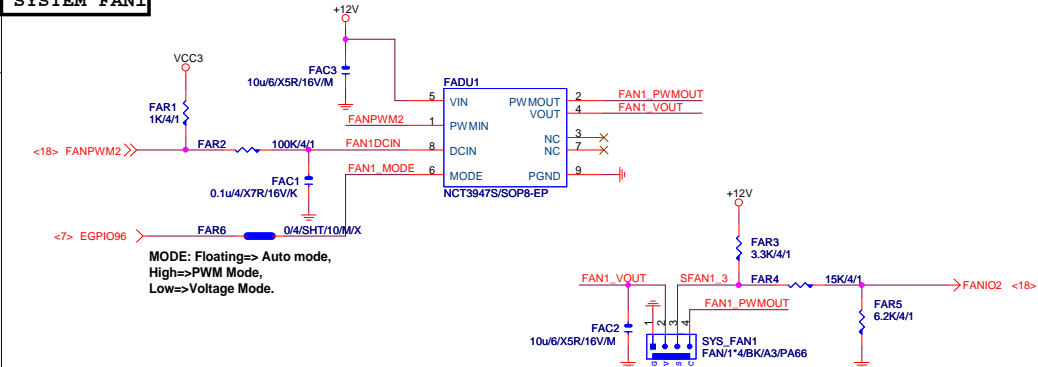
			
Title			
DDR PWR, 5VDUAL, 3VDUAL			
Size	Document Number	Rev	
Custom	B450 AORUS PRO WIFI	1.01	
Date:	Friday, September 21, 2018	Sheet 28 of	B450 AORUS PRO

I211AT不支援:NC-SI,SMBus

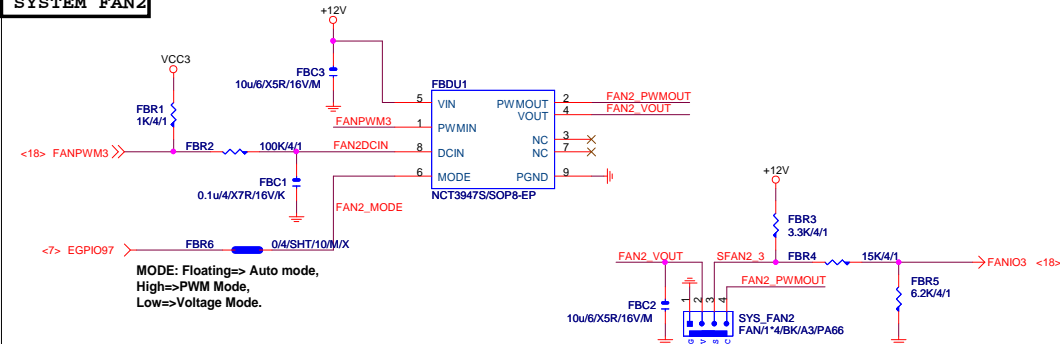




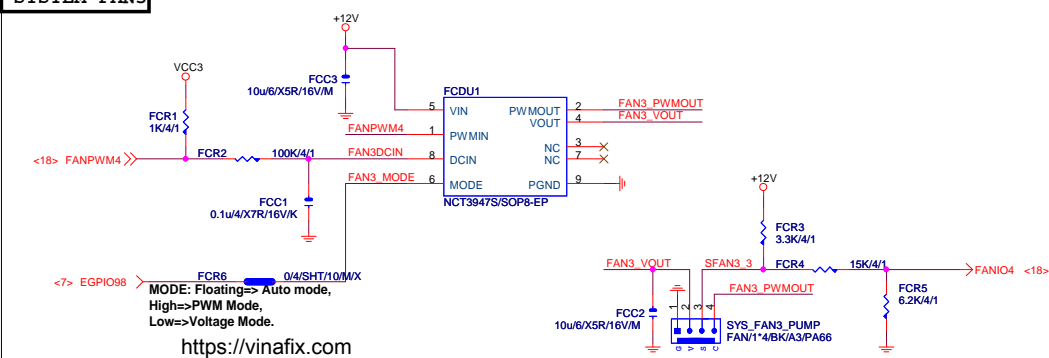
SYSTEM FAN1



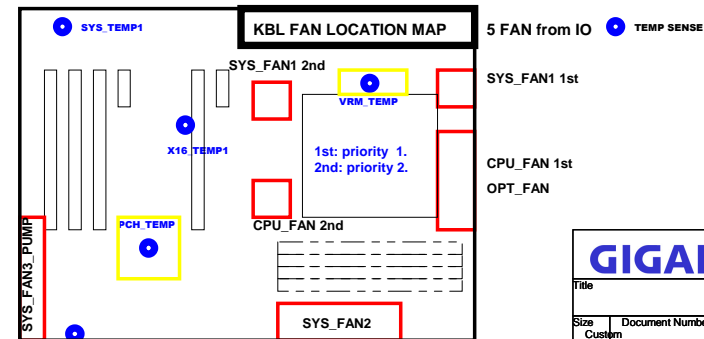
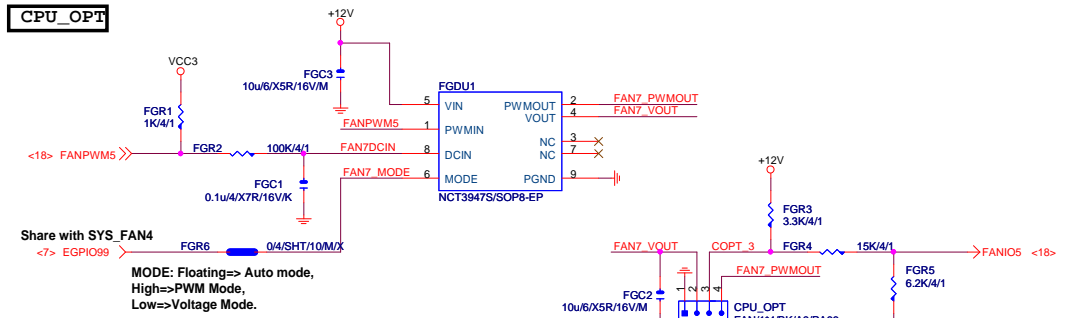
SYSTEM FAN2



SYSTEM FAN3



CPU_OPT



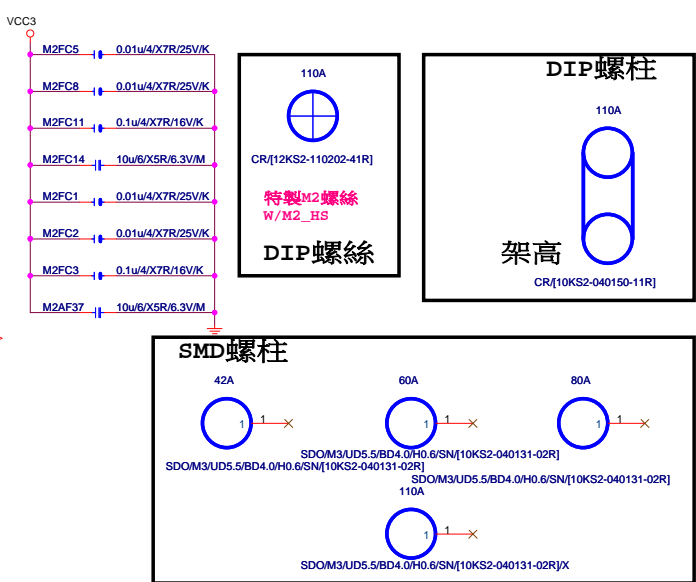
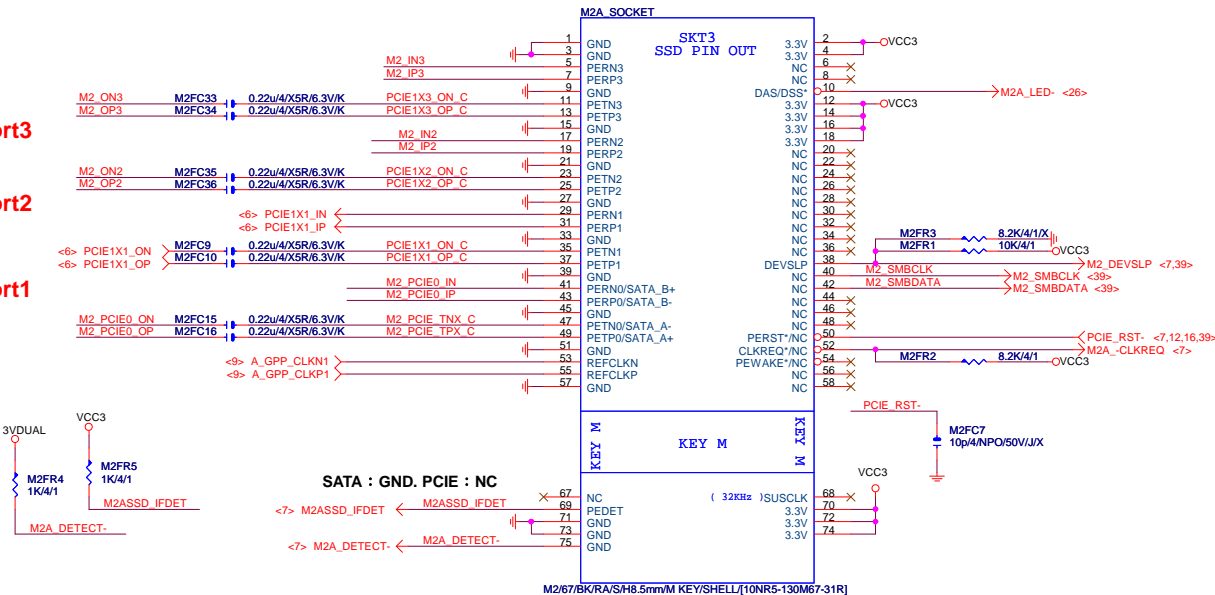
Rev 0.5

M.2 Lane4 from AM4 port3

M.2 Lane4 from AM4 port2

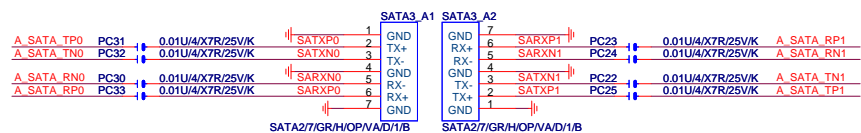
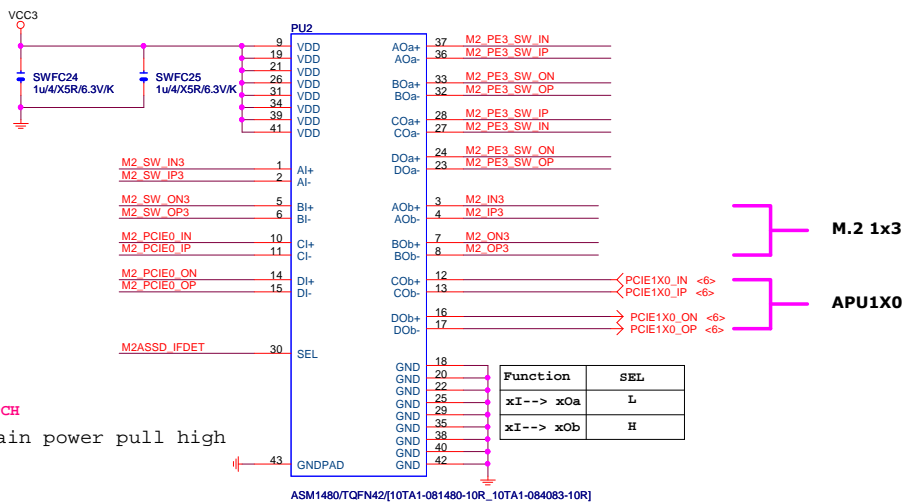
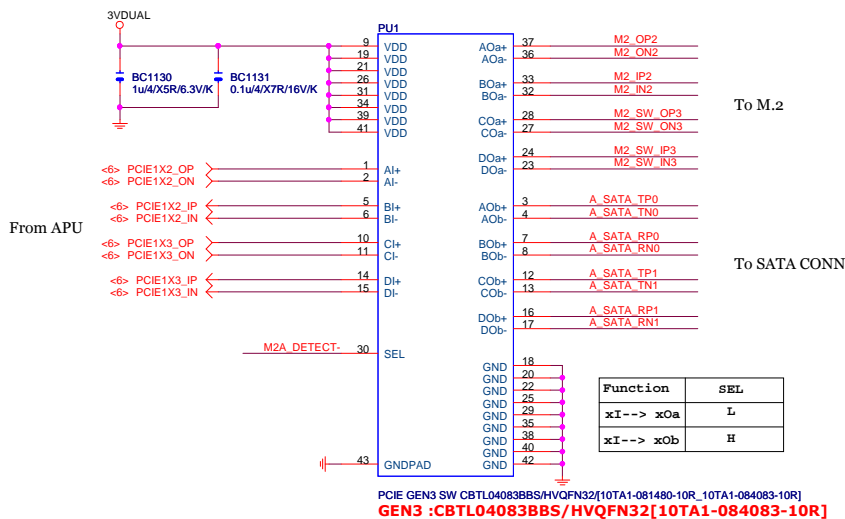
M.2 Lane4 from AM4 port1

by SWITCH Select



teknisi-indonesia.com

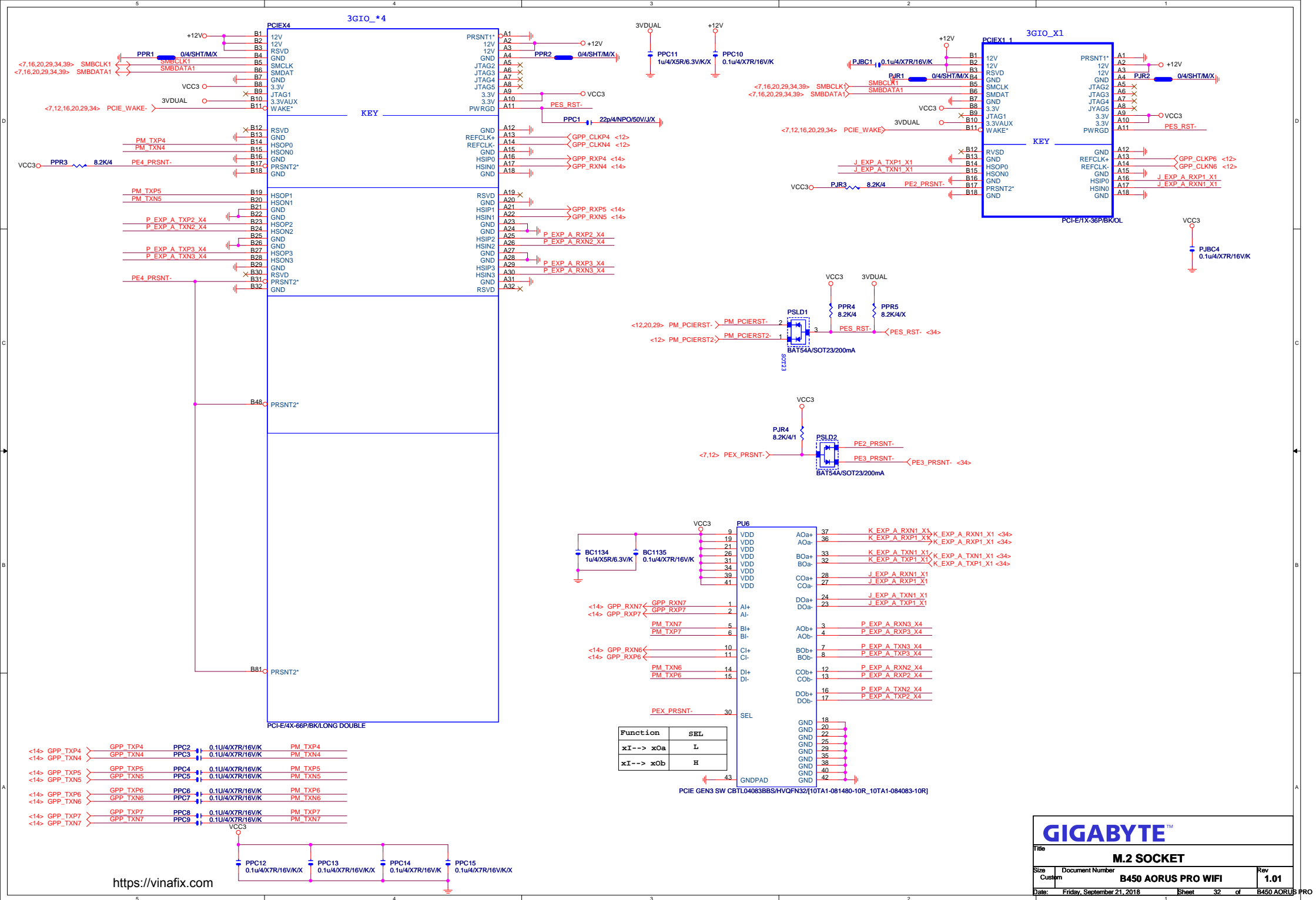
8.5H鐵殼
Footprint :M2_110(DIP)

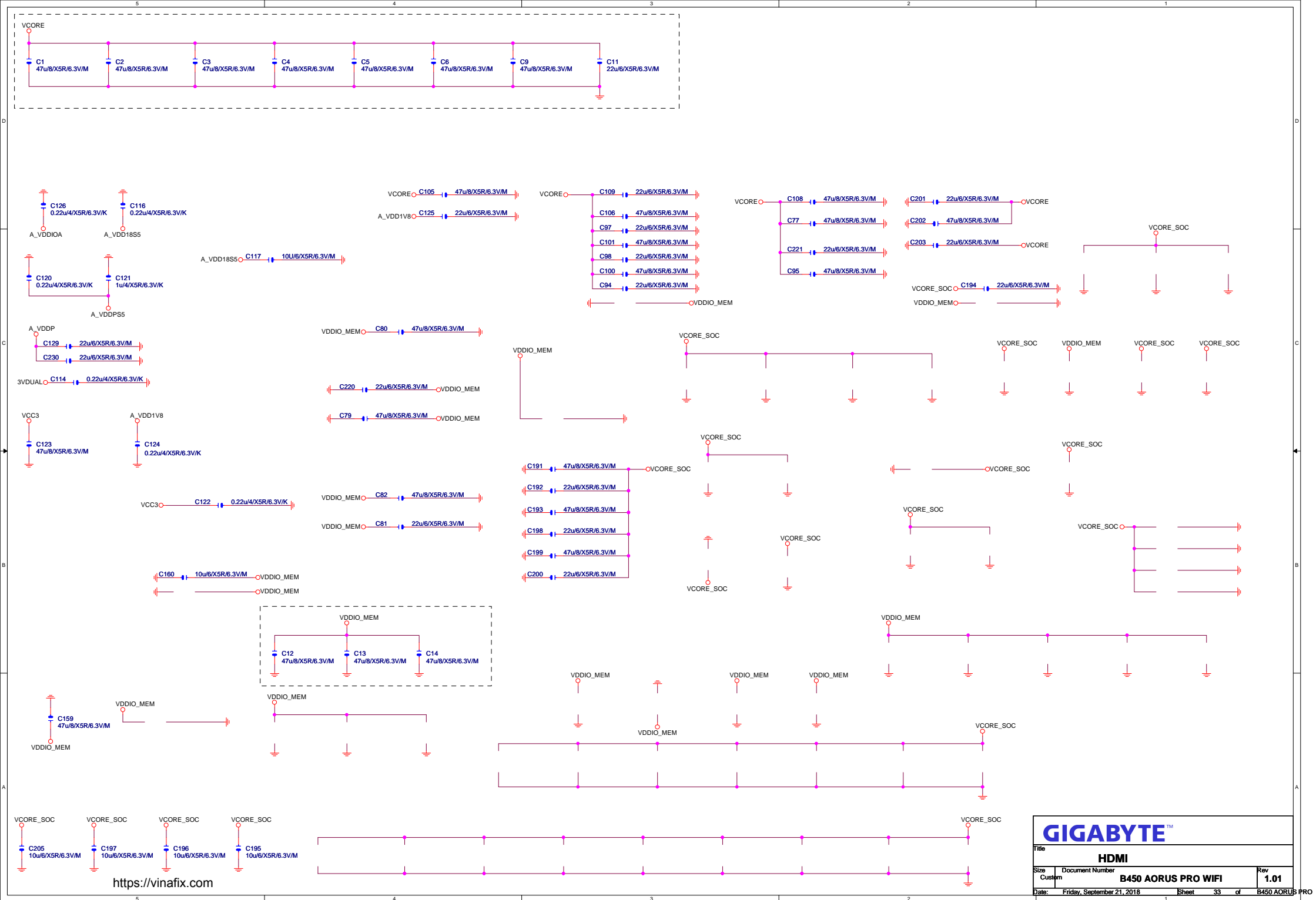
M2A_SOCKET
M2A_SOCKET_HS[12SP1-S10205-32R_12SP1-S10205-33R] **M2 HEATSINK**

<https://vinafix.com>

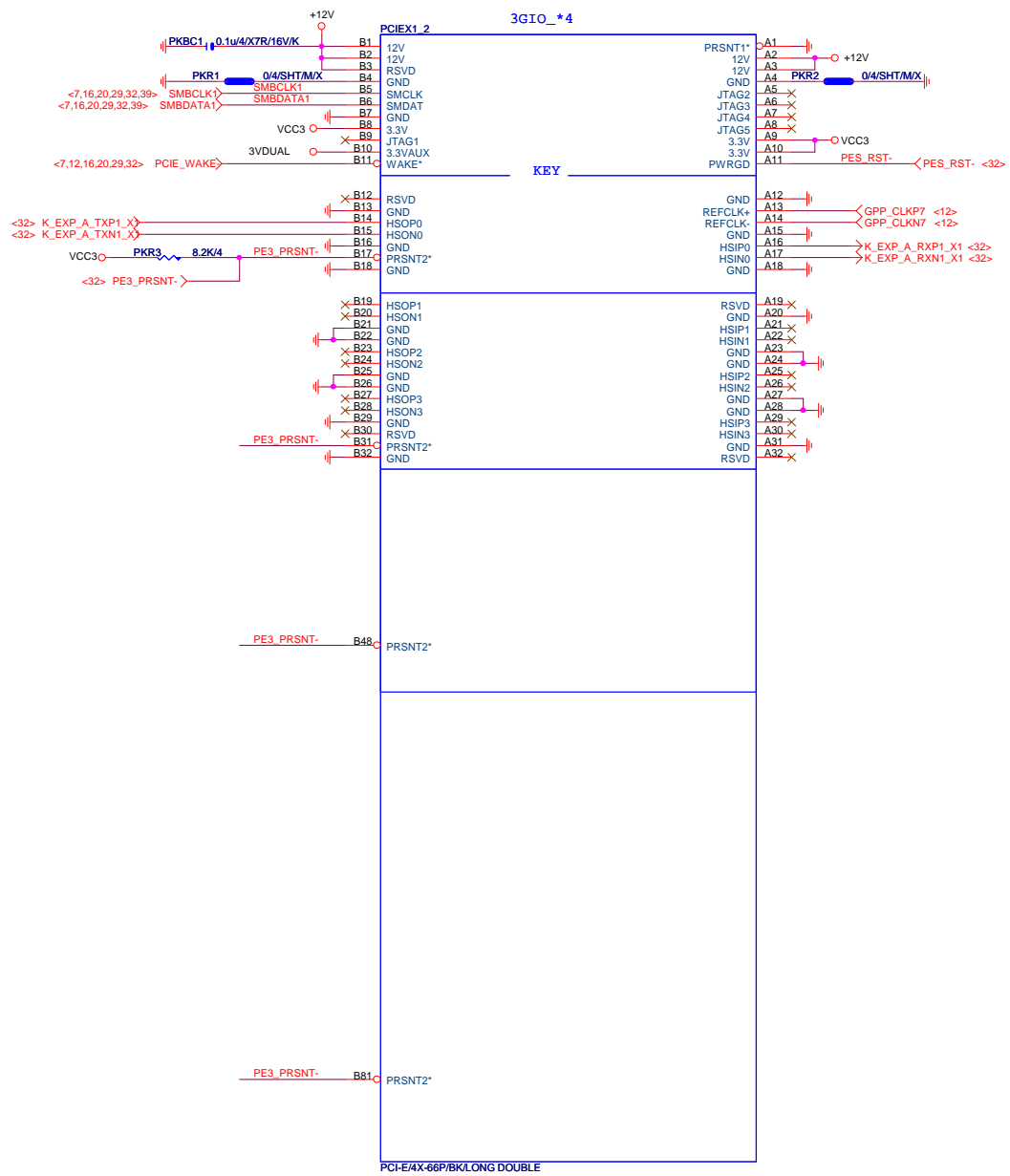
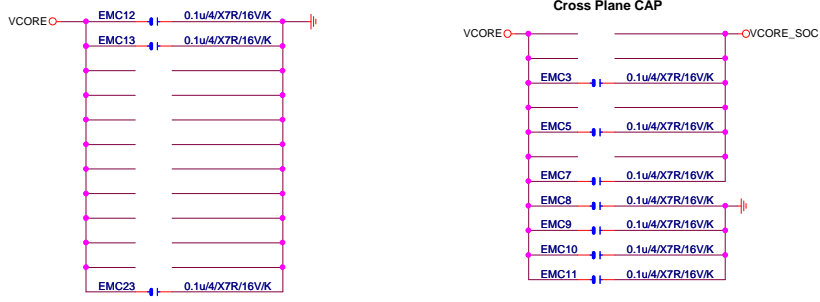
GIGABYTE

Title			
M.2 SOCKET			
Size	Document Number		Rev
Custom	B450 AORUS PRO WIFI		1.01
Date:	Friday, September 21, 2018		Sheet 31 of B450 AORUS PRO





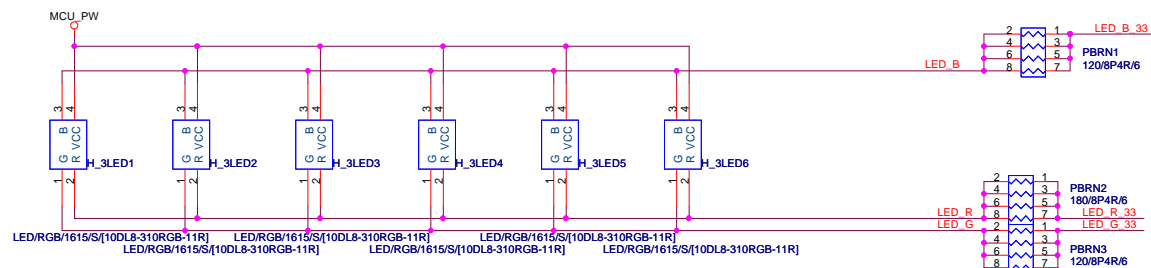
CPU TOP CAVITY



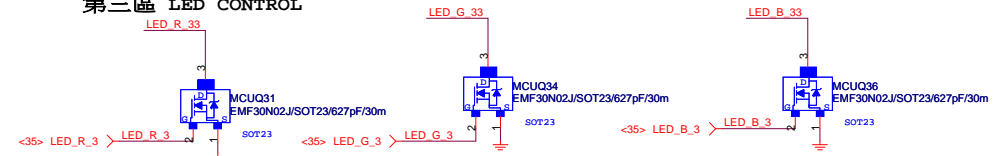
GIGABYTE™			
Title HDMI			
Size Custom	Document Number B450 AORUS PRO WIFI	Rev 1.01	
Date: Friday, September 21, 2018	Sheet 34 of 34	B450 AORUS PRO	

第三區 LED

FOR PCH 正發光 LED*6 (位置在正板,依據PCH_HS設計擺放)



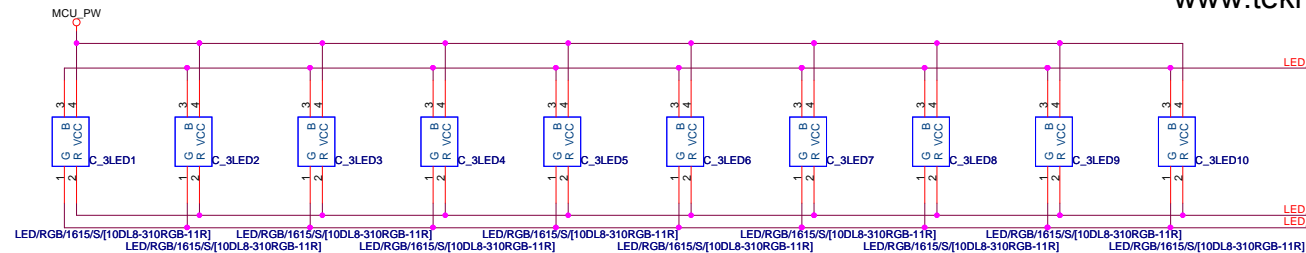
第三區 LED CONTROL



RGB LED壓克力燈條 REMOVE

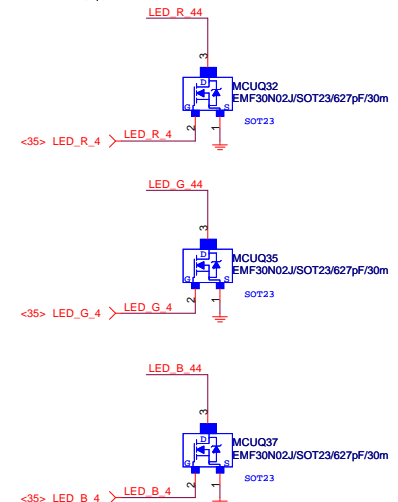
第四區 LED

FOR AUDIO 正發光 LED*10 C_3LED1~10)

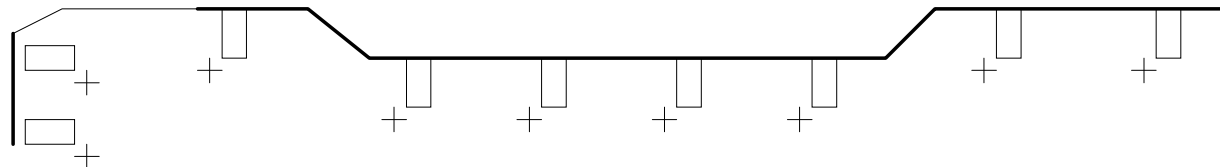


www.teknisi-indonesia.com

第四區 LED CONTROL



Audio Ground切割線+背面 RGB LED

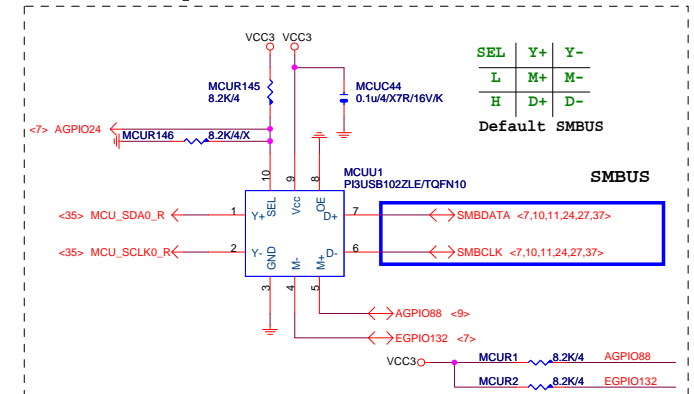


RGB LED LAYOUT 注意事項：

1. Debug LED (各LED依CPU/DRAM/VGA/BOOT個別位置擺放)
2. 背板 RGB LED 方向整板請統一如下
(整板正極可統一朝下或朝上)
3. 正板 RGB LED 統一方向即可
4. MCU_PW & MCU_PW33電源一律走20mils
5. ECF1, ECF2, ECF3, ECF5 兩端電源走80mils或用鋪銅方式加粗
6. MCU LED 出pin的走線4mils,如:LED_R_1,LED_G_1,LED_B_1
7. LED RGBW rule :W/S=10/5 mils 如:LED_R_11,LED_G_11,LED_B_11,LED_W.....
(包含從晶體到排阻到LED的net)
8. Digital LED NET rule W/S=4/8 mils
GPD0_SDA_B,GPD0_SDA_BB,GPD0_SDA_C,GPD0_SDA_CC

https://vinafix.com

For AMD MCU update

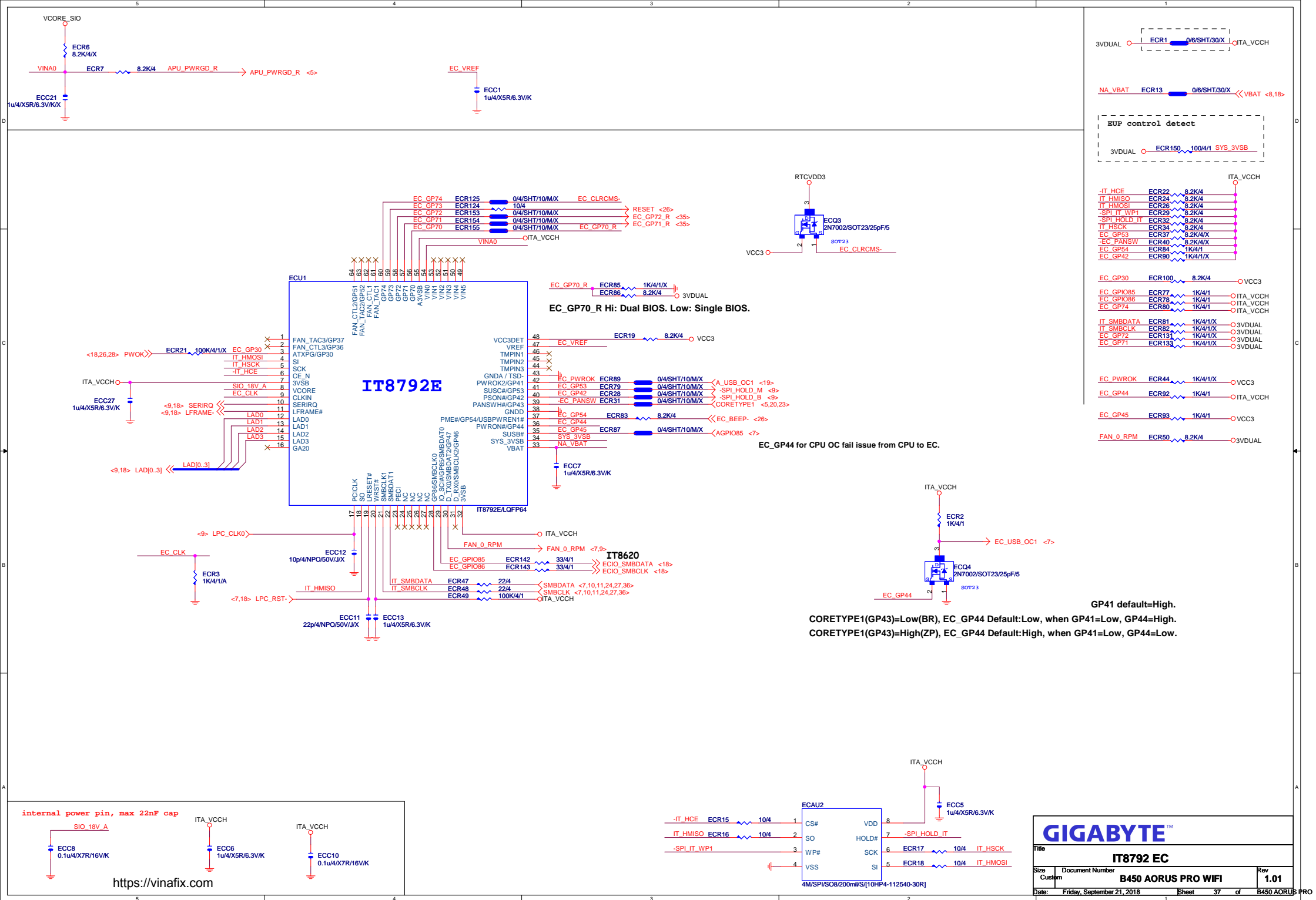


GIGABYTE™

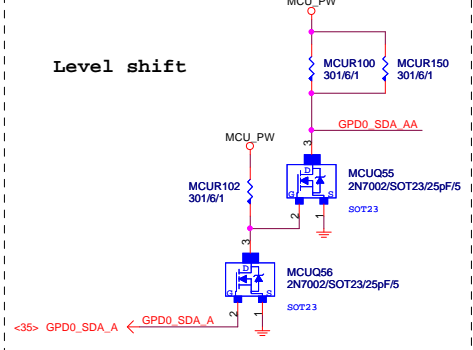
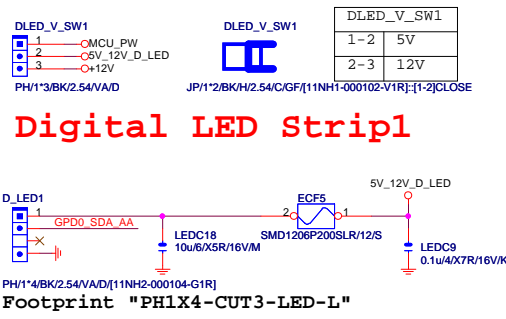
Title PCB / PCH / DDR / LED_C LED

Size Custom Document Number B450 AORUS PRO WIFI Rev 1.01

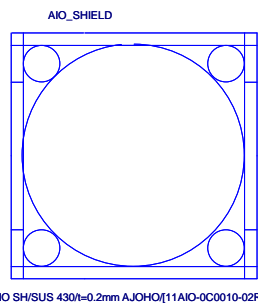
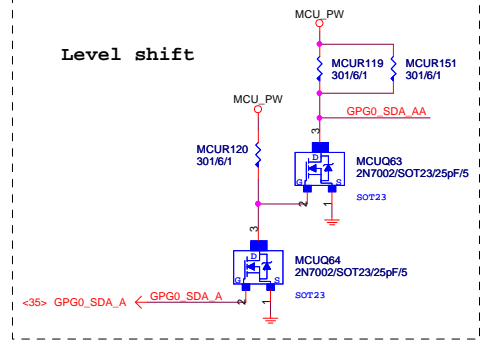
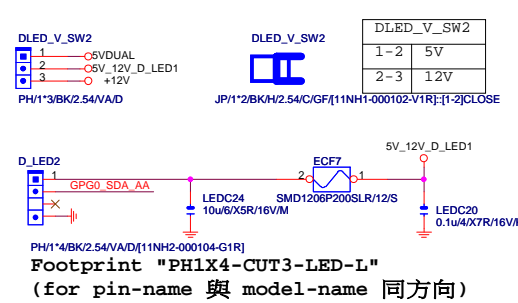
Date: Friday, September 21, 2018 Sheet 36 of B450 AORUS PRO



第六區 LED (靠近左上板邊位置)



第七區 LED (靠近右下DDR板邊位置) Digital LED Strip2



Rev 0.5



BIOS設為main power pull high



To SATA CONN

Function	SEL
xI--> xOa	L
xI--> xOb	H

